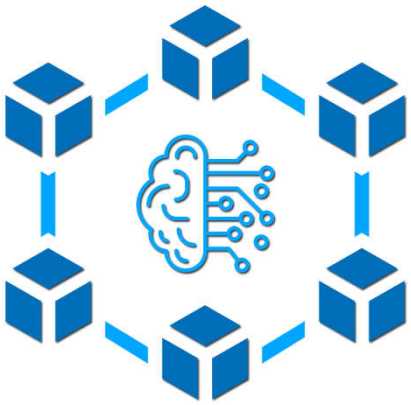

An Artificial Intelligent Aided Unified Network for Secure Beyond 5G Long Term Evolution [GA: 101096456]

Deliverable 6.4

In-lab testbeds definition

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List of Acronyms

Acronym	Explanation
AI	Artificial Intelligence
AMF	Access and Mobility management Function
B-RAN	Blockchain Radio Access Network
B5G	Beyond Fifth Generation
CPUs	Central Processing Units
CoMP	Coordinated Multi-Point
COTS	Commercial Off-The-Shelf
CUPS	Control and User Plane Separation
DX.Y	Deliverable X.Y
DoW	Description of Work
eNB	Evolved Node B
EPC	Evolved Packet Core
E2SMs	E2 Service Models
FPGA	Field Programmable Gate Array
GA	Grant Agreement
gNB	Next Generation Node B
IoT	Internet-of-Things
I/O	Input / Output
KPI	Key Performance Indicator
KVI	Key Value Indicator
ML	Machine Learning
MAC	Medium Access Control
MEC	Multi-access Edge Computing
MEAO	Mobile Edge Application Orchestrator
MIMO	Multiple-Input Multiple-Output
MME	Mobility Management Entity
mmWave	millimetre Wave
NG-SON	Next-Generation Self-Organizing Networks
NAS	Non-Access Stratum
NFVO	Network Functions Virtualization Orchestrator
NUC	Next Unit of Computing
O-RAN	Open Radio Access Network
ONF	Open Networking Foundation
ONOS	Open Networking Operating System
OTF	On-The-Fly
PDCP	Packet Data Convergence Protocol
PGW	Packet data network GateWay
PPI	Pixels Per Inch
QoS	Quality of Service
RAN	Radio Access Network
RF	Radio Frequency
RRC	Radio Resource Control

RLC	Radio Link Control
RT RIC	Real-Time Radio Intelligent Controller
RUs	Radio Units
SISO	Single-Input Single-Output
SoC	System-on-Chip
SGW	Serving GateWay
SLA	Service Level Agreement
SMF	Session Management Function
SIM	Subscriber Identity Module
SDRAM	Synchronous DRAM
SLC	Single-Level Cell
SSD	Solid-State Drive
SDK	Software Development Kit
SDR	Software-Defined Radio
SubX	Sub-scenario X
TX.Y	Task X.Y
TOPS	Tera-Operations-Per-Second
UE	User Equipment
UPF	User Plane Function
USB 3.0	Universal Serial Bus 3.0
VNFs	Virtual Network Functions
WP	Work Package

Executive summary

The present document incorporates detailed descriptions of all the necessary equipment and individual components entailed for operating the two in-lab testbeds. The primary objectives are to conduct a complete preliminary evaluation of the testbeds, define how they operate, and propose a comprehensive operational design. This deliverable will establish two in-lab testbeds to undertake detailed analysis and execution.

The information in this deliverable will lay the foundations for Task 6.5 - “Greek in-lab testbed” and Task 6.7 - “Italian in-lab testbed”, which coincide with the implementation of the Greek and Italian in-lab testbeds, respectively. This document emphasizes the necessity of understanding each testbed's requirements, including the underlying information, resources, and data required to ensure that the testbeds are being carried out effectively. A detailed review of these requirements serves as a solid basis for the deployment of the testbeds. There are detailed explanations of all the hardware required for the testbeds, including both generic and specialized equipment for data collection and processing. The document divides each testbed meticulously into its individual components, delivering useful insights. As a result, it is easier to establish critical roles and responsibilities, the implementation process is streamlined, and an in-depth understanding of the testbeds' details is facilitated. Furthermore, the importance of establishing well-defined, unambiguous objectives for each testbed in order to ensure collaboration among participants and effective progress monitoring. The present document underlines the significance of building an ordered structure for the testbeds' activities, in addition to the technological requirements.

In summary, this deliverable is essential to the two in-lab testbeds' smooth operation as it goes into the testbed details, ensuring that everyone participating is prepared to take part in accomplishing the intended objectives. To achieve the goals of the testbeds in an effective and efficient manner, it is necessary to cultivate clarity and rigorous planning.

1. Introduction

NANCY's envisioned output is the development of B5G prototypes and testbeds that incorporate the project's novel concepts, with the ultimate goal of stimulating future commercialization of Beyond Fifth-Generation (B5G) products and services based on these concepts described and developed throughout the NANCY project's life cycle. To achieve this goal, NANCY emphasizes the significance of building two indoor testbeds, one in Greece and one in Italy, respectively. The main responsibilities of WP6 include the detailed implementation and development of those two pilots. WP6 is especially in charge of system integration, demonstration, and validation planning. In order to achieve those objectives, D6.4 – "In-lab testbeds definition" will initiate the process of producing detailed planning reports for the two in-lab NANCY testbeds (Greek, Italian) that will be developed and used for the Blockchain Radio Access Network (B-RAN) modelling and experimentally verifying the theoretical framework of NANCY presented at WP2, in real-world conditions. In addition, D6.4 – "In-lab testbeds definition" focuses particularly on providing the plan and specifications for the aforementioned in-lab testbeds.

- **The Italian in-lab testbed** delivers data anticipated from WP2 to demonstrate the B-RAN modelling and achieve the objectives of examining its performance and verification of the NANCY theoretical framework in the Coordinated Multi Point (CoMP) scenario (i.e., usage scenario 1: fronthaul network of fixed topology) - Figure 1: . As a result, all parameters derived from the experimental activities will be incorporated once again into WP2 with the objective of constructing an accurate B-RAN model and experimentally proven analytical framework. On top of that, edge anomaly detection and offloading functionalities will be presented and reviewed thoroughly.

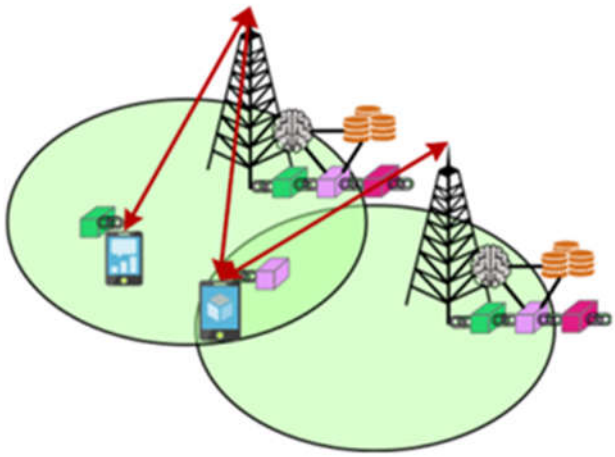

Figure 1: Usage Scenario 1: Fronthaul network of fixed topology

- **The Greek in-lab testbed** encompasses the critical WP2 data for the B-RAN modelling to evaluate its performance and verify the developed theoretical framework of NANCY within the scope of the range expansion scenario (i.e., usage scenario 2: advanced coverage expansion) - Figure 2: . Additionally, the outcomes of the experimental activities will be incorporated into WP2.

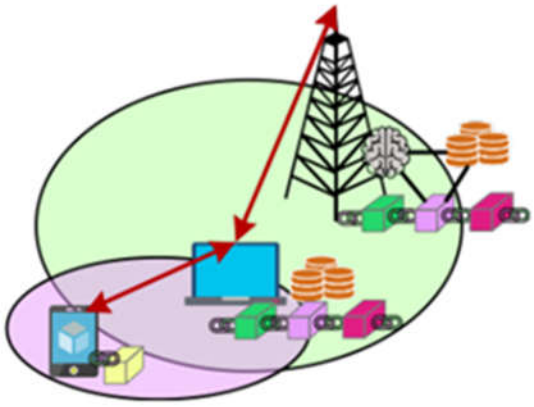

Figure 2: Usage Scenario 2: Advanced coverage expansion

In conclusion, it is important to highlight that both testbeds are mobile; consequently, they will be utilized to showcase NANCY's most important achievements and capabilities at conferences and other events.

1.1. Purpose of the Document

This deliverable reports the in-lab testbeds plan and specifications. Specifically, D6.4 – "In-lab testbeds definition" incorporates the required preparation procedures that are essential for the operation of the two in-lab testbeds.

1.2. Relation to other Deliverables

The relations of this deliverable with other deliverables of the NANCY project are illustrated in Figure 3: Relation to other deliverables. D6.4 – "In-lab testbeds definition", primarily interconnects with two corresponding Work Packages (WPs) of the NANCY project, namely WP2 and WP3. Regarding WP2, it receives input from D2.1 – "NANCY Requirements Analysis" as has been described in detail in the project's Grant Agreement (GA). D2.1 – "NANCY Requirements Analysis" provides a general overview of the NANCY Use Cases (UCs) that will be employed in the two in-lab testbeds. NANCY will utilize the reference architecture described at WP3, which will serve as a baseline architecture for the usage scenarios covered in each pilot conducted by NANCY. As a final step, the outcomes of D6.4 – "In-lab testbeds definition" will subsequently contribute to D6.5 – "Greek in-lab testbed dataset 1", D6.7 – "Greek in-lab testbed dataset 2", D6.6 – " Italian in-lab testbed dataset 1", D6.8 – " Italian in-lab testbed dataset 2" which will emphasize further on the development of Greek and Italian testbed, respectively.

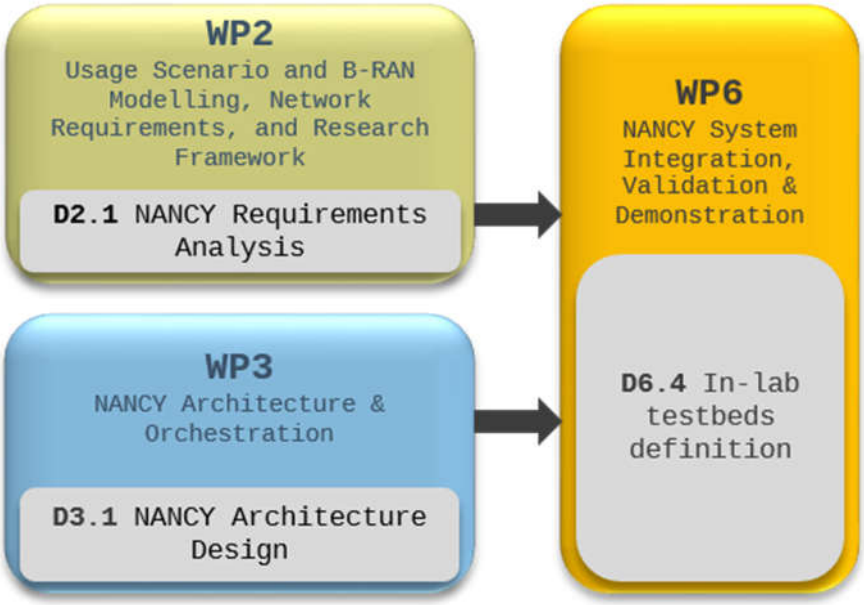

Figure 3: Relation to other deliverables

1.3. Structure of the Deliverable

The deliverable is organized as follows:

- **Section 1 - Introduction:** This section provides an introduction to the deliverable.
- **Section 2 - NANCY Reference architecture:** This section presents the NANCY reference architecture and specifically its initial release which serves as a baseline architecture for the usage scenarios that will be covered at each demonstrator of the NANCY project.
- **Section 3 - In-lab Testbed Requirements and Specifications:** This section covers the requirements, components, setup, and activities, and describes a detailed plan regarding the in-lab testbeds.
- **Section 4 - Evaluation Methodology and outcomes:** This section presents the data that have been collected from the two testbeds.
- **Section 5 - Conclusion:** This section concludes the deliverable.
- **Appendix:** In this section, the components of the in-lab testbeds are described in detail.

2. NANCY Reference Architecture

The Open Radio Access Network (O-RAN) initiative is a global effort that proposes novel architectural transformations for the RAN. The initiative seeks to introduce virtualized network elements, openness, and intelligence to RAN management, with the aim of leveraging the potential of Machine Learning (ML) and network virtualization in next-generation communications. O-RAN has been recognized as a significant facilitator for RAN sharing, as it allows for the deployment of multiple vendors through the dynamic management and coordination of radio and cloud resources, while also integrating Artificial Intelligence (AI) capabilities [1]. The design of O-RAN presents novel opportunities for operators to facilitate the delivery, distribution, and implementation of Virtual Network Functions (VNFs). In order to satisfy the demands of UE, stakeholders can expeditiously procure and deploy VNFs through catalogues, commonly referred to as marketplaces. Service providers who have resources on their website are able to openly disclose their service terms and pricing, enabling other participants to select the most favourable option. Under this approach, the competition remains unregulated while the pricing structure remains fixed and does not cater to the individual requirements of RAN users. In light of the O-RAN's open sharing contexts, it is imperative to employ distinct methodologies that facilitate secure and dependable dynamic and real-time competitive resource trading.

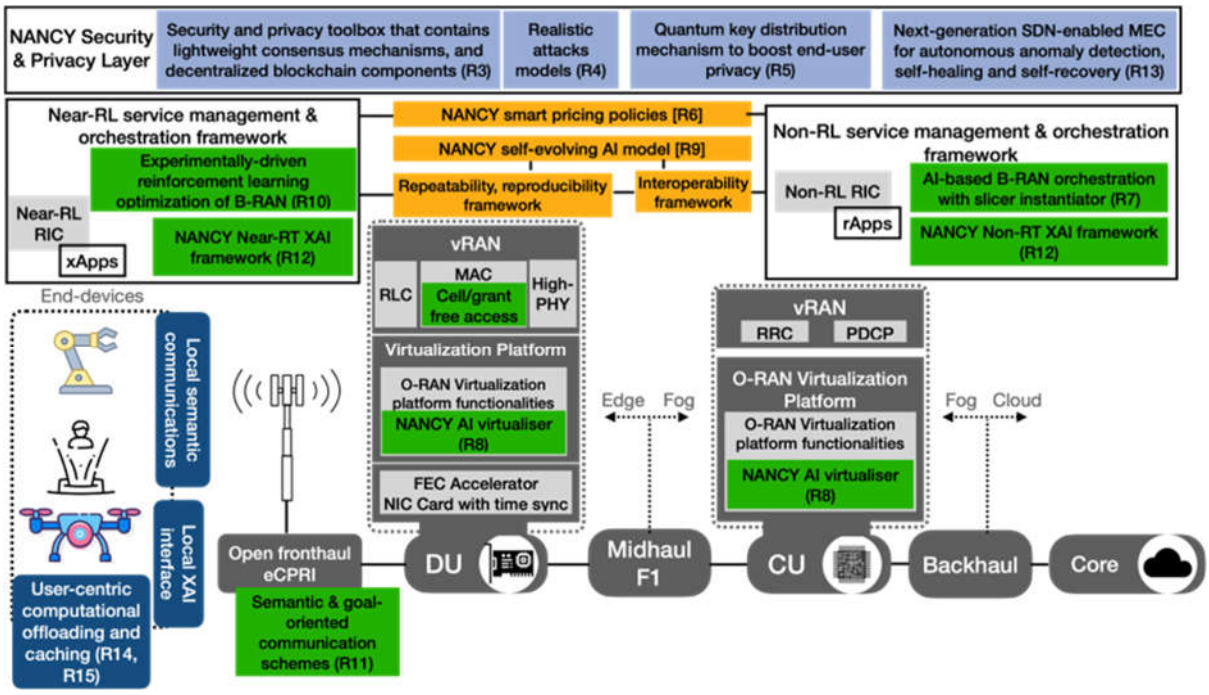

Figure 4: NANCY reference architecture.

In order to facilitate the advancement and bolster the assurance of these novel open markets, NANCY intends to integrate blockchain and smart contract technologies into the O-RAN Medium Access Control (MAC) layer. This integration will furnish indelible and enduring records that are amenable to scrutiny by relevant stakeholders. The utilization of a smart contract facilitates the elucidation of the requirements of the RAN user and the implementation of the Service Level Agreement (SLA). The utilization of Next-Generation Self-Organizing Networks (NG-SON) and O-RAN results in enhanced automation and network management efficiency. Furthermore, the integration of blockchain technology obviates the requirement for costly intermediaries such as banks and credit rating agencies, while also providing unparalleled levels of transparency and reliability, thereby offering the possibility of substantial cost reductions. In addition, blockchain reduces the duration required to achieve consensus, thereby facilitating seamless RAN sharing. In B5G networks, O-RAN is considered a

fundamental architecture. Operators utilize B-RAN sharing to dynamically sublease their resources, thereby capitalizing on pre-existing infrastructure and enabling other operators to augment their coverage and capacity. Operators have the liberty to opt for the most optimal equilibrium between capital investment and resource utilization at any given point in time, irrespective of whether they are entering into a RAN sharing agreement or implementing a network. The facilitation of democratization and decentralization in the telecommunications industry is made possible by the implementation of dynamic resource trading. This mechanism enables the emergence of novel competitive marketplaces, featuring new providers.

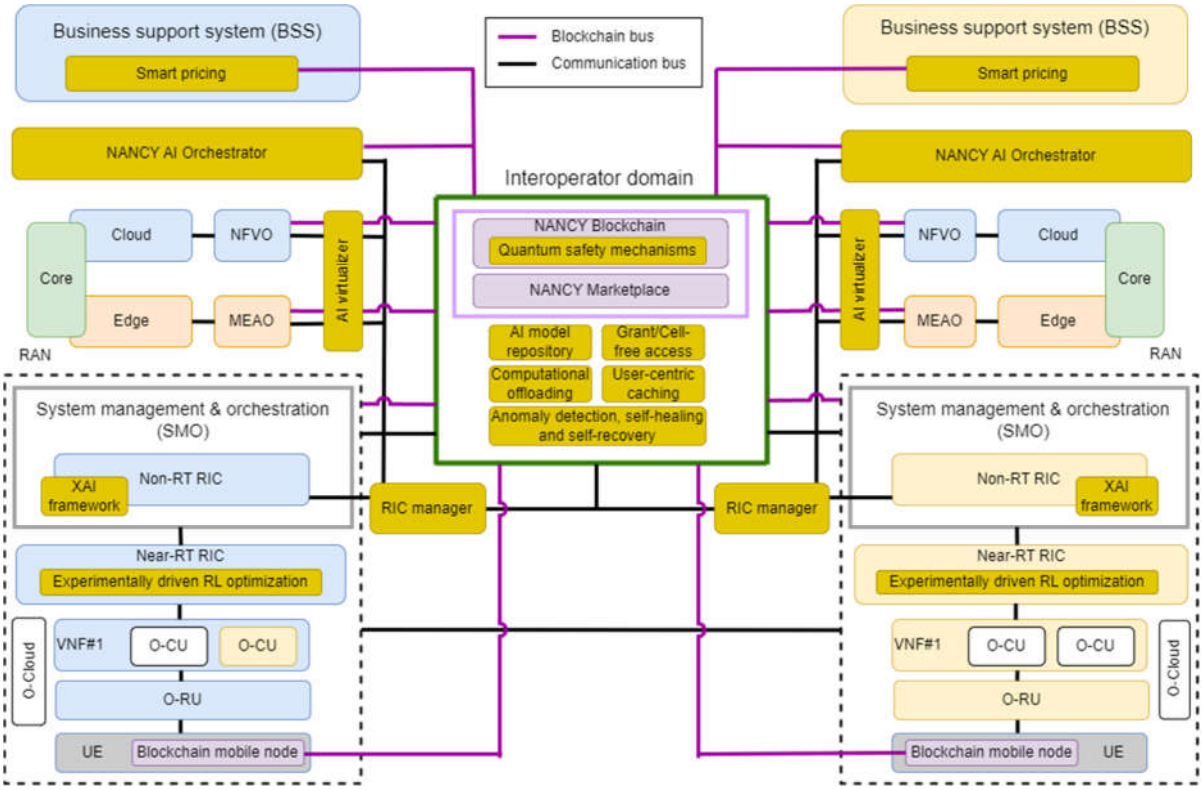

Figure 5: Interconnections of NANCY network architecture.

The design of the NANCY network at a high level is shown in Figure 5. The presented architecture spans across the edge-to-cloud continuum. The edge is managed by the Mobile Edge Application Orchestrator (MEAO), while the cloud is ruled by the Network Functions Virtualization Orchestrator (NFVO). In addition, the RAN part is shown in black dashed line and is built upon the O-RAN architecture. The NANCY components are visually distinguished by the colours purple and yellow, representing the blockchain and network aspects, accordingly.

The blockchain serves as the fundamental technology behind NANCY, allowing the different components of the platform to access it via either i) Post Quantum Cryptography (PQC) in the case of User Equipment (UE) or ii) blockchain adaptors in the case of the orchestrators. The marketplace resides together with the blockchain and makes available both resources and prices for all interested actors. Both the blockchain and the marketplace are located inside the interoperator domain, which serves as the core area of the NANCY architecture, where the components of NANCY are located and used by several operators. The components included in the interoperator domain are the AI model repository, compute offloading, user-centric caching, quantum safety, grant/cell-free access, anomaly detection, self-healing, and self-recovery procedures.

In order to maintain continuous connection and smooth movement of UE, a number of mobile relay nodes are deployed to create multi-hop networks. This guarantees the transmission of data between different network nodes, assures the dependability of the network, and provides connectivity even in difficult conditions. The network architecture facilitates wireless connectivity for both stationary and mobile devices. A comprehensive control and pricing system, which integrates blockchain systems and intelligent pricing rules, enables interoperability, security, trust, and efficient resource management. This partnership improves user experience and fosters collaboration among operators.

NANCY seeks to address the challenges in conventional O-RAN topologies by including cell-free access, multi-hop networking, and relay nodes. This methodology enhances the allocation of resources, synchronization, and scalability, enabling operators to flexibly modify the quantity of RAN nodes as required. Multi-hop networks effectively reroute traffic to appropriate RAN nodes, hence preventing congestion. Operators cooperate to provide uninterrupted communication between nodes, while blockchain technology will be used for secure transactions and authentication. This connection will also facilitate the implementation of sophisticated strategies for the allocation and distribution of resources.

In recent years, several open-source cellular systems for 5G Standalone (SA) have surfaced. These systems offer a chance for the research community to collaborate with the industry in practical experiments and promote standardization and optimization efforts for 5G SA technology. There are three prominent 5G RAN projects that are widely recognized in the scientific community, namely OpenAirInterface[1] (see Appendix 2: OpenAirInterface, srsRAN[2], and UERANSIM[3]. Both OpenAirInterface and srsRAN have been developed to incorporate a specific subset of Release 16 of the 3GPP standard. In contrast to these, UERANSIM solely incorporates Layer 3 radio protocols, specifically the Radio Resource Control (RRC) and Non-Access Stratum (NAS) layers. It does not encompass Layer 1, which pertains to the physical layer, nor does it include Layer 2, encompassing the MAC, Radio Link Control (RLC), and Packet Data Convergence Protocol (PDCP) layers of the RAN protocol stack. Since srsRAN and OpenAirInterface offer a comprehensive implementation of the entire protocol stack that aligns with the 3GPP standards[4] and specifications for 5G networks, they are the most promising implementations for NANCY.

The primary distinction between srsRAN and OpenAirInterface is in the numerical representation of sub-carrier bandwidth, the number of channels, and the availability of supporting documentation. The utilization of OpenAirInterface offers increased adaptability in the allocation of sub-carrier bandwidth. This enhanced flexibility allows for reduced latency and facilitates the provision of support for higher-frequency bands, particularly in the context of larger bandwidths, such as the mmWave spectrum. While srsRAN is limited to operating with Single Input Single Output (SISO) antenna configurations, OpenAirInterface has the capability to support both SISO and Multiple Input Multiple Output (MIMO) channels. Despite OpenAirInterface exhibiting a higher level of maturity in relation to its range of features, srsRAN has superior comprehensive documentation and community support, hence facilitating a more streamlined deployment process. Based on the aforementioned rationales, NANCY will use srsRAN as an initial step toward the exploration and enhancement of 5G network research.

The integration, demonstration, and evaluation of key technologies and functionalities within an ecosystem. To verify, assess, and exhibit the viability, suitability, efficiency, profitability, and limitations

[1] https://openairinterface.org/
[2] https://www.srsran.com/
[3] https://opencollective.com/UERANSIM
[4] https://www.3gpp.org/specifications-technologies/releases

of the NANCY architecture across various wireless settings, two in-lab testbeds will be provided. The demonstrators are expected to utilize the technological advancements achieved in WP4 and WP5 as well as the demonstration scenarios defined in D2.1 – “NANCY Requirements Analysis”. The prototypes will be developed utilizing the prototyping equipment offered by the primary partners participating in the project, who have already received internal authorization from their respective headquarters to supply such equipment. Furthermore, the deployment of each testbed will be led by UOWM and ITL, who will evaluate its functionality and commercial viability from a business standpoint.

3. In-lab Testbed Requirements and Specifications

As the cornerstone for meeting the objectives set by the NANCY project, the establishment of the in-lab testbeds, which will take place in Greece and Italy, is essential to the development and validation of the innovative B5G concepts and prototypes that have been implemented across the span of the project. The present document delves into detail on the technical integration and implementation of these testbeds in the following section 3. Specifically, it focuses on the multitude of ways whereby the Italian and Greek in-lab testbeds immensely enhance B-RAN modelling and the theoretical framework verification of the project. In addition, a detailed analysis will be implemented starting with providing the testbeds requirements (subsection 3.1.1 and 3.2.1), focusing particularly on their corresponding usage scenarios that are outlined in this document's first section. To further ensure that the testbeds are operated in accordance with the project's objectives, an in-depth review of the hardware and software requirements will be presented as well (subsections 3.1.2, 3.2.1), thus encompassing a thorough analysis of the (software and hardware) components utilized in each of these two pilots. Furthermore, subsections 3.1.3 and 3.2.3 will investigate the complicated nature of each testbed configuration, going into detail on both the software and network layers. Within this framework, an in-depth view of the proposed layout associated with each testbed will be illustrated via graphical representations. Moreover, the following subsections 3.1.4 and 3.2.4 will describe the experimental plans for every testbed, including the tasks that will be carried out and the practical aspects of using these testbeds to validate and progress the project's objectives. In the final part of section 3, the planning of each testbed activities will be outlined, with the goal of improving, optimizing, and providing the final NANCY system performance assessment.

3.1. Greek in-lab Testbed

The following subsections provide the details and features of the Greek in-lab testbed. A cutting-edge testbed for the range expansion scenario of B-RAN modelling, performance evaluation, and theoretical framework validation will be examined in detail. Additionally, as the testbed is located in a laboratory environment at UOWM's premises, all the experimental conditions can be monitored and configured in detail.

3.1.1. Testbed Requirements

The aim of the Greek in-lab testbed is to assess the B-RAN performance in the context of 'Usage Scenario 2: Advanced Coverage Expansion' and validate the NANCY advancements in a controlled laboratory environment. Moreover, the testbed will be leveraged for the creation of two versions of datasets (i.e., D6.5 and D6.7 - Greek in-lab testbed dataset 1 and 2).

Specifically, multi-hop connectivity, which is evaluated in this testbed, is a network communication strategy where data traverses through a series of intermediary nodes, or hops, to bridge the gap between the source and the destination. This chain of nodes can include various devices such as routers, relays, base stations, and mobile devices, each serving as a pivotal link in the communication chain. The multi-hop approach is particularly advantageous in situations where obstacles like physical obstructions, signal degradation, or extensive distances impede direct communication lines. Through the strategic positioning of these intermediary nodes, multi-hop connectivity ensures that data can be relayed effectively, maintaining communication continuity even in less-than-ideal conditions.

The software infrastructure plays a pivotal role in orchestrating the complex interactions between hardware components within a multi-hop network. To evaluate the B-RAN architecture in this testbed, the software must support the decentralized nature of blockchain, ensuring secure and transparent

data transactions across the network. Network management platforms are essential for maintaining efficient data routing, real-time network optimization, and the execution of smart contracts that are part of the blockchain's logic. These platforms also facilitate the dynamic allocation of network resources, a core feature of the O-RAN architecture. Security protocols are integral to safeguarding data integrity and privacy, a non-negotiable aspect of blockchain systems. Testing tools are also crucial, as they allow for the emulation of various network scenarios to evaluate the performance and resilience of the B-RAN setup, ensuring that the network remains robust, adaptable, and secure under different conditions.

The hardware infrastructure for a multi-hop network, especially one designed to test a blockchain-based O-RAN architecture, must be both resilient and adaptable. These components are chosen for their robustness and capacity to meet the network's specific demands, which are critical for both O-RAN and blockchain operations. The inclusion of diverse user equipment reflects the range of devices interacting with the network while computing resources like servers and edge devices provide the processing and storage resources needed to support the computational intensity of blockchain transactions and O-RAN's intelligent management.

3.1.2.Testbed Components

The Greek In-lab testbed is located on the premises of UOWM. The hardware aspect of the testbed consists of:

A. The following equipment will be used for setting up two private 5G networks:
   1. Ettus Research USRP X310 (see Appendix 6: USRP X310 and UBX 160 USRP Daughterboard), equipped with two UBX160 daughterboards.
      - 2x2 MIMO channels.
      - Up to 160 MHz bandwidth.
      - Supports frequencies from 70 MHz to 6GHz.
   2. Ettus Research USRP B210 (see Appendix 7: Ettus Research USRP B210)
      - 2x2 MIMO channels.
      - Up to 56 MHz bandwidth.
      - Supports frequencies from 70 MHz to 6GHz.
   3. Two high-performance laptops.
      - Intel i7 12-thread & Intel i7 20-thread CPUs.
      - 16 & 32 GB of RAM

B. The following equipment will act as UE devices that will connect to the 5G network and generate network traffic:
   1. Quectel RM520N-GL 5G Module: This module is connected to a laptop through a USB adaptor.
   2. SIM8200A-M2 5G Hat: This module is mounted on a RaspberryPi, equipping it with 5G connection capabilities.
   3. Xiaomi 11 Lite 5G NE Mobile Phone
   4. Sysmocom sysmoISIM-SJA2 subscriber identity modules (SIMs) that are inserted in the UE.

Concerning the software aspect of the testbed the following tools will be deployed:

1. The Open5GS (see Appendix 1: Open5GS) and OpenAirInterface 5G Core Network (see Appendix 2: OpenAirInterface) software is responsible for serving the 5G Core functionalities to the Base Stations.

2. The srsRAN (see Appendix 3: srsRAN) and OpenAirInterface 5G RAN (see Appendix 2: OpenAirInterface)software is used for managing the USRPs and configuring them as gNB nodes.
3. The SD-RAN (see Appendix 4: SD-RAN) and FlexRIC (see Appendix 5: FlexRIC) software will be used as a basis for the O-RAN architecture.

The hardware utilized in the Greek in-lab testbed is depicted in Figure 6: Greek in-lab testbed hardware. a) High performance laptops, b) USRP X310, c) USB Dongle with Quectel 5G Module, d) USRP B210, e) SIM8200A-M2 5G Hat, f) Mobile Phone.

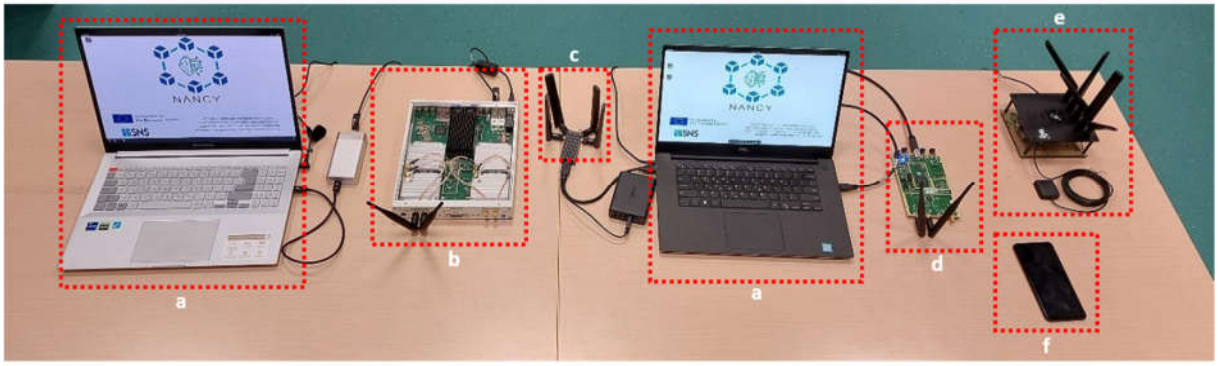

Figure 6: Greek in-lab testbed hardware. a) High performance laptops, b) USRP X310, c) USB Dongle with Quectel 5G Module, d) USRP B210, e) SIM8200A-M2 5G Hat, f) Mobile Phone

3.1.3.Testbed Configuration

The details of the testbed configuration are covered in this subsection. The aforementioned hardware, software, and interfaces for each device component (see subsection 3.1.2) are displayed qualitatively in Figure 7: Greek in-lab testbed topology, which provides an in-depth breakdown of the topology of the testbed. This section offers crucial details about the fundamental design which underpins the experimental framework.

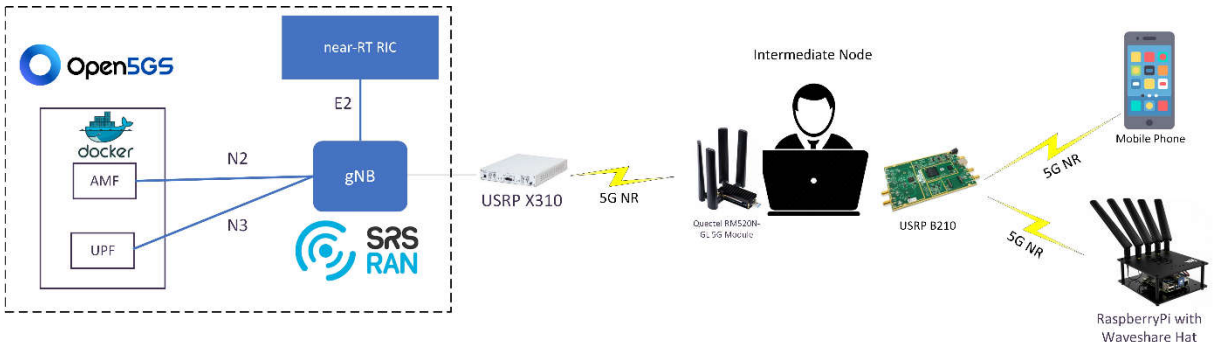

Figure 7: Greek in-lab testbed topology

The gNB, acting as the 5G base station (BS), is responsible for managing the radio protocol stack's lower layers, ensuring connectivity to UE devices, such as a mobile phone or a 5G-enabled Raspberry Pi. The near-Real-Time RAN Intelligent Controller (near-RT RIC) directly interfaces with the gNBs through the E2 interface, conforming to O-RAN specifications. This controller is pivotal in managing and optimizing the RAN elements, providing enhanced efficiency and real-time responsiveness.

Open5GS takes on the role of the core network, delivering essential functions such as the AMF, SMF, and UPF through N2 and N3 interfaces. It orchestrates control-plane and user-plane traffic, ensuring smooth session management and mobility across the network.

To investigate multi-hop connectivity, the testbed also includes an intermediate node, for which the high-performance laptop is utilized, between the RAN and core network components. The Quectel RM520N-GL 5G module is connected via USB to the laptop to offer 5G connectivity.

A Raspberry Pi, equipped with a SIM8200A-M2 5G Hat, and a Xiaomi 11 Lite 5G NE mobile phone act as user equipment extending the testbed's capabilities and enabling a range of connectivity and testing operations in the context of 5G. This versatile setup can generate traffic, establish a backhaul connection, or function as a test controller or data logger for diverse testing scenarios.

This testbed topology, with its interconnected components, facilitates comprehensive testing of 5G technologies. It allows for the investigation of complete functionalities, such as quality of service (QoS) testing, and overall connectivity, all within the O-RAN architecture.

3.1.4.Experimental Activities

The experiments that will take place in the Greek in-lab testbed involve two scenarios, namely A) a scenario in which all UE devices are corrected directly to the BS, and B) a scenario in which an intermediate node is used to provide coverage to the UE devices. The two scenarios are depicted in Figure 8.

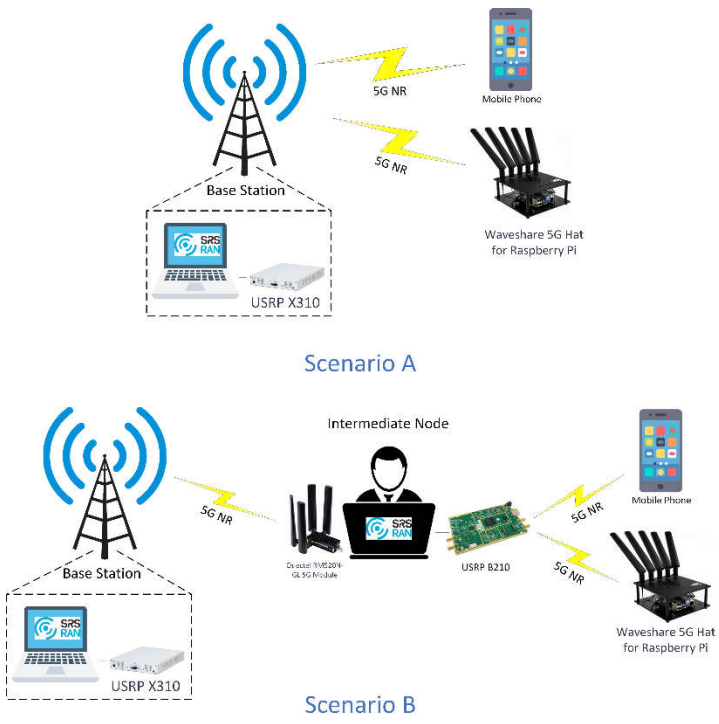

Figure 8: Experimental Activities in the Greek In-lab testbed

The main aim of the experimental facilities in the Greek in-lab testbed is to evaluate the energy consumption of the BS and the UEs, as well as the overall security level of the considered network architecture. To this end, a video streaming application will be employed. In general, streaming applications require the transmission of large data volumes with very low latency. Therefore, they are useful assets for evaluating and assessing the network performance in real time. Furthermore, other

traffic generation tools, such as the iperf[5] and nping[6] tools, will be employed for creating additional network traffic.

In more detail, the video streaming application and the traffic generation tools will run in both scenarios and the respective network performance metrics will be assessed (e.g., latency, power consumption, jitter, etc.). The self-recovery/healing and caching are two aspects that will be also investigated in the Greek in-lab testbed. Specifically, the intermediate node may become unavailable (for instance, when the node is turned off or is compromised due to a cyberattack). In addition, a moving device may need to disconnect from the BS and connect to the intermediate node for energy-efficiency reasons. To ensure a constant stream of video data, the handover between the BS and the intermediate node will have to take place with minimum delay.

3.2. Italian in-lab Testbed

The following subsections demonstrate a testbed for Usage Scenario 1: "Fronthaul network of fixed topology – Direct Connectivity & Coordinated Multi Point (CoMP)" for B-RAN modelling, performance measurement, and theoretical framework validation, similar to the Greek in-lab testbed previously addressed. The implementation of the testbed, in an indoor environment, located in Italtel's (ITL's) premises at Milano, provides regulated and measured experimental conditions, enabling accurate data collection and analysis. Additionally, comprises tools for anomaly identification and unloading, which allow further augmentation of the overall network performance evaluation.

3.2.1.Testbed Requirements

This subsection addresses the requirements emanating from Usage Scenario 1: "Fronthaul network of fixed topology – Direct Connectivity & Coordinated Multi Point (CoMP)", in the context of testbed requirements. These requirements are a manifestation of the valuable input received from Tasks 2.1 – "Use Case Definitions, Network Requirements Specifications and Technology Enablers" and 2.2 – "Experimental-driven B-RAN and Attacks Modelling". Particular emphasis is lavished on both hardware and software components, with a focus on the underlying infrastructure, to ensure the successful operation of the Italian in-lab testbed.

VOS' will target the deployment of VNFs to ARM-powered edge servers through its low-overhead virtualization technology. Thanks to the proximity of these VNFs to the UE and to the lightweight virtualization solution, we aim to deploy an application function that will be a good test bench for the latency-related Key Performance Indicators (KPIs). In this context, a fitting application function will be identified and customized for the demonstrator. As of now, a video streaming application seems to be a good candidate. The targeted deployment will rely on the AI Virtualiser which encompasses the Slice Manager to orchestrate the deployment of the application function to the edge server.

Related to the hardware requirement, VOS will identify an ARM-powered board suitable for edge-oriented workloads. Once the board is identified and at VOS' disposal, it will be integrated into Italtel's indoor testbed at the Caldera Park site. At the time of writing, the identified ARMv8 board as a candidate target for NANCY is the Texas Instrument SK-AM69 (see Appendix 8: Texas Instruments SK-AM69).

3.2.2. Testbed Components

[5] https://iperf.fr/
[6] https://nmap.org/nping/

The Italian In-lab testbed relies on the infrastructure available at ITL's indoor lab, in Caldera Park (Milano) site. The Italian in-lab testbed relies on an open and flexible configuration, which allows the integration of other hardware and/or software components in case the progress of NANCY development activities requires it.

Below there are two images of the current Italtel indoor lab, with the components set up for the Italian in-lab testbed:

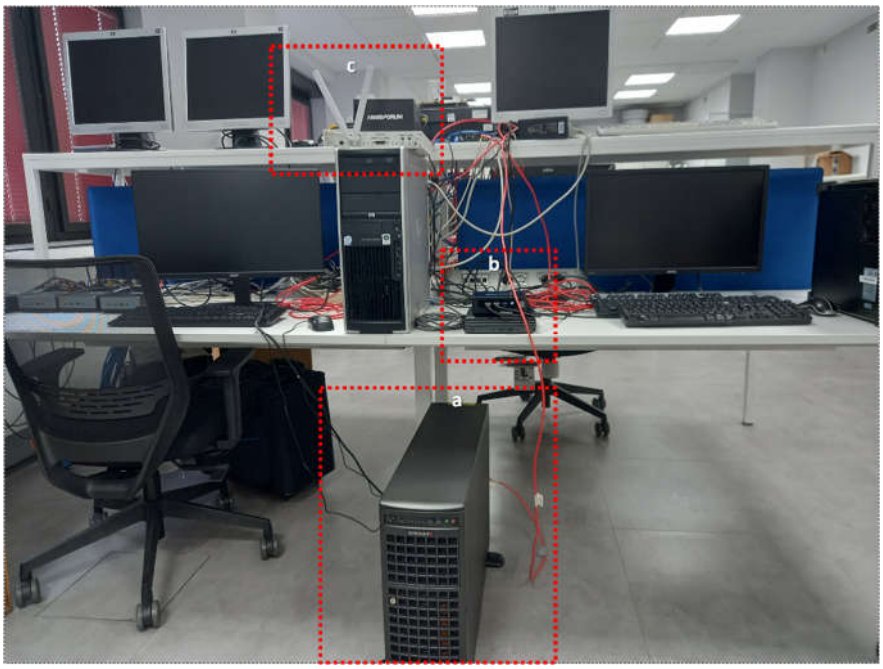

Figure 9: NANCY's Italian in-lab testbed - picture 1: a) GPU SuperServer SYS-741GE-TNRT + 2 GPU NVIDIA A40, b) Intel® NUC, c) USRP X310

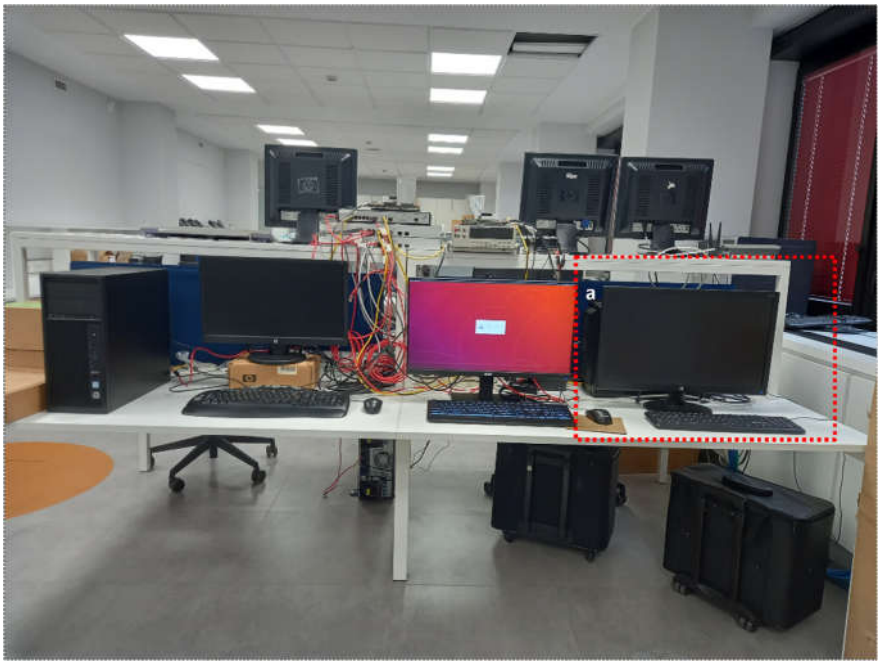

Figure 10: NANCY's Italian in-lab testbed - picture 2: a) MEC Host - portable

In detail, the Italtel indoor lab consists of:

- a MEC Host, an Edge server integrating a GPU (NVIDIA P4), as hardware accelerator to increase performance (portable), configured as follows:
  - Mainboard with 2x PCI-E 3.0 x16, 2 PCI-E 3.0 x8,
  - 2 x Intel® Xeon® Silver 4114, 10 Core, 2.2 – 3.0 GHz,
  - 128GB DDR4 ECC memory,
  - 1 x 256GB 2.5" SSD for OS (boot disk) removable,
  - 1 x 1TeraByte 2.5" SSD, (storage) removable,
  - GPU NVIDIA P4 (Low Profile, 75W, PCIe 16x),
  - NIC Mellanox ConnectX-4 Lx EN NIC, 10GbE single-port SFP28,
  - 2x USB3.0, 2x USB2.0, 2x LAN GbE.
- a GPU SuperServer SYS-741GE-TNRT + 2 GPU NVIDIA A40:
  - 4th Gen Intel® Xeon® Scalable processor support, including Xeon® CPU MAX Series;
  - 4TB disk, 128GB DRAM Memory Type: 4800MHz ECC DDR5;
  - Up to 4x double width, full length GPUs; 4x PCIe 5.0 x16 (double-width) slots, 3x PCIe 5.0 x16 (single-width) slots;
  - 2x M.2 NVMe for boot drive only; Up to 8x NVMe drives (8 NVMe drives supported by default); Total 8x 3.5" Hot-swap SATA/NVMe/SAS drive bays;
  - 4 Removable heavy duty fans w/ Optimal Fan Speed Control;
  - 2x 2000W (1+1) Redundant Power Supplies, Titanium Level;
  - 4 network interfaces 1G
- an Intel® NUC (see Appendix 10: Intel® NUC);
- Ettus X310 2xUBX160 board (USRP X310 High Performance Software Defined Radio - Ettus Research);
- 5G terminal with eSIM (Google Pixel7 Android 5G, Moto G100), (see Appendix 9: Google Pixel7 Android 5G, Moto G100);
- an open 5G RAN system, using open-source software (5g-srsRAN Project - Open source 4G/5G software suites developed by Software Radio Systems, running on an Intel® NUC, and Open5GCore running on an intel-based server). In any case, depending on the requirements coming from the project, a different option can also be considered, if necessary, and integrated.
- An ARM v8/v9 edge server with TrustZone extension and Gigabit connectivity. This edge server, provided by Virtual Open System (VoS) project partner, will rely on an external USRP device that provides 5G connectivity. The ARMv8 board identified as candidate target for NANCY is the Texas Instrument SK-AM69 evaluation boards.

srsRAN, developed by SRS, is an open-source software solution that runs on top of both x86-based personal computers (PCs)/servers and ARM CPUs (e.g., Raspberry Pi) for virtualized 4G and 5G networks. The srsRAN[7] project codes are hosted on GitHub. Furthermore, SRS offers a software platform for 5G UE emulation, facilitating detailed simulations of packet transmissions between a network and UEs.

3.2.3. Testbed Configuration

The figure below shows the Italian in-lab testbed equipment and high-level configuration:

[7] https://github.com/srsran

Figure 11: Italian in-lab testbed equipment and high-level configuration

The aforementioned hardware and software, along with the interfaces are shown in **Error! Reference source not found.**, which depicts the testbed topology and configuration.

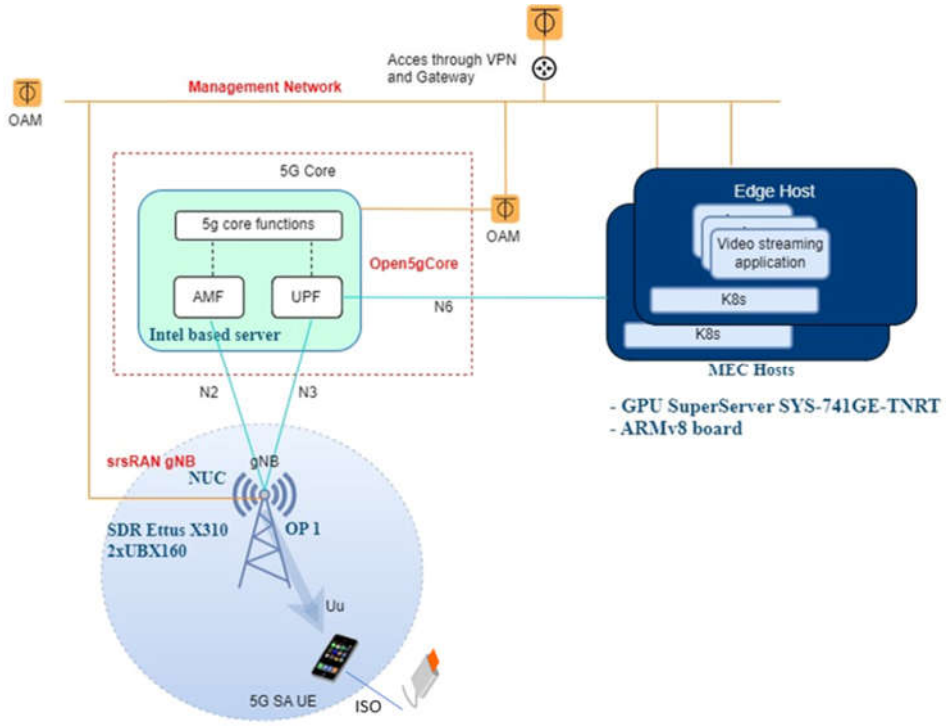

Figure 12: Italian in-lab testbed topology and configuration

The interfaces highlighted in the figure are:

- **Uu**: this interface connects the gNB and the NR-UE over the air
- **N2**: this interface connects gNB and the AMF. Due to Control and User Plane Separation (CUPS), before a service can be accessed, the UE must be connected to the network. This interface is used for all control plane signalling.
- **N3**: this interface connects the NG-RAN and the UPF. In this case, this interface carries user information.
- **N6**: This interface provides connectivity between the UPF and Data Network, any internal or external network such as clouds or internet.
- **ISO**: This interface connects UE to the PQC signature Token.

3.2.4. Experimental Activities

One of the activities of the Italian in-lab testbed can be the video streaming use case mentioned in Section 3.2.1, which allows the evaluation of various parameters by analysing the statistics of the video streaming.
The figure below shows each network segment relevant to the measurements:

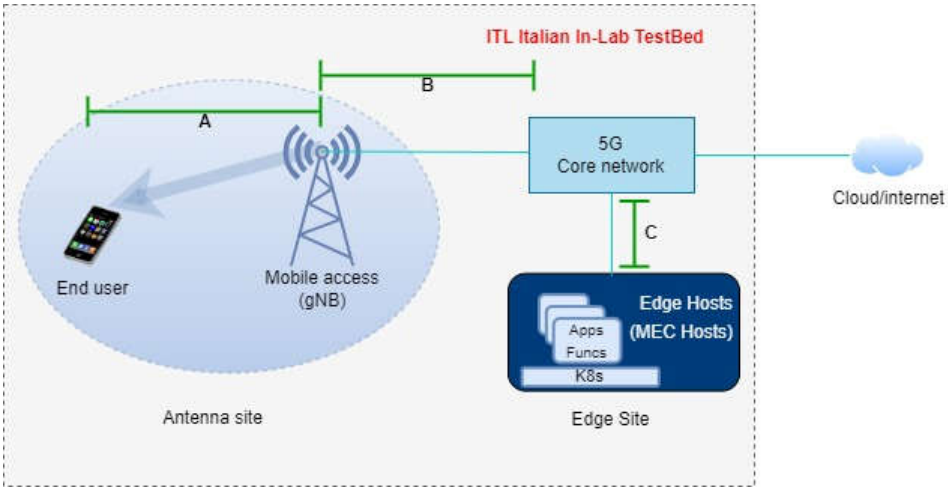

Figure 13: Italian In-lab testbed: network segments for measurements - A, B and C

A Video Streaming Application has been selected since, as an example, there are some major challenges associated with video streaming services: The specific challenges are analysed by Khan *et al.* and listed below, with limitations on bandwidth, latency, and jitter being identified as the primary obstacles in offering customers with continuous data globally [2]. Particularly:

- **Limited Bandwidth**: More data rates are available over cellular links with contemporary 5G networks; nonetheless, bandwidth restrictions are becoming more common since greater video material with significantly higher resolutions is utilised. The 4K (3840 × 2160), 8K (7680 × 4320), and 360° videos that are now accessible can be classified as bandwidth-intensive. For instance, a 60-frame 4K video utilizes 1 to 10 GB of data per minute, while a 20-minute 4K video uses approximately 100 GB.
- **Latency**: Latency affects the streaming of videos in general and live streaming in particular. Many applications, including virtual reality, online gaming, and live streaming of 4K and 8K films, are negatively impacted by the increased latency results, thus providing an inferior user experience.
- **Jitter**: The undesired divergence of an anticipated periodic signal from its genuine periodicity is commonly referred to as jitter or delay variation. Furthermore, variations in scheduling intervals and queuing might trigger jitters.

3.3. Activities Planning

The following section analyses the planning methodology that we employed to specify and organize our project's activities. It includes an in-depth breakdown of the procedures adopted in order to plan, organize, and implement the different activities that are necessary for the successful completion of both in-lab testbeds.

To define the planning of the activities of T6.5 – “Greek in-lab testbed”, and T6.7 - “Italian in-lab testbed”, the following aspects are considered:

- the Milestones directly linked to testbeds' activities;
- as well as the relationship between the testbeds and other Tasks of the project that, in some way, are interconnected to the experimentations that will be fulfilled in each testbed;
- Finally, the plan of the expected project results that are linked to both testbeds' activities.

Therefore, in drawing up the plan, it is worth mentioning that strong coordination with the partners leading the aforementioned tasks is necessary. Moreover, some updates to the plan may be also necessary, as the project progresses.

In consideration of the above, the planning (initial draft) of testbeds' activities is split into two different macro plans and defined as follows: "Datasets' (1 & 2) generation plan" and "Plan of the activities related to the project's results achievement".

The first one – "Datasets' (1 & 2) generation plan **"–** foresees the following steps:

1. **Design phase - testbed requirements definition:** The requirements come from T2.1 "Use case definitions, network requirements specifications and technology enablers", in particular those linked to the range expansion scenario and CoMP scenario, for Greek in-lab testbed and Italian in-lab testbed, respectively, and related UCs, and from T2.2 "Experimental-driven B-RAN and attacks modelling". This phase is preliminary to the preparation of both testbeds.
2. **Release cycle 1:** it is composed of the activities to configure and set up the scenarios in each of the testbeds, including installation of software applications developed in the project, if and when necessary.
3. **Experimental activities - cycle 1 (as detailed in 3.1.4 and 3.2.4):** these activities will produce the experimental data expected from T2.2 to train the ML models.
4. **First Evaluation:** Feedback, software updates, and bug fixes.
5. **Data set 1 generation:** completion of deliverables D6.5 – "Greek in-lab testbed dataset 1" and D6.6 – "Italian in-lab testbed Data set 1", in M12; D6.5 and D6.6 are the means of verification of MS3 "Availability of NANCY in-lab testbeds".
6. **Release cycle 2:** the aim of this phase is to take into account any possible changes to the test environment, coming from the project's progress; it is composed of the same type of activities as the Release cycle 1.
7. **Experimental activities - cycle 2 (as detailed in 3.1.4 and 3.2.4);** these activities will produce the experimental data expected from T2.4 "Performance Assessment via Modelling and Testbed Results".
8. **Final updates and bug fixes**.
9. **Dataset 2 generation:** completion of D6.7 – "Greek in-lab testbed dataset 2" and D6.8 – "Italian in-lab testbed dataset 2", and the respective Milestones 5 and 6 "Availability of NANCY Greek/Italian in-lab testbed dataset 2" in M21.

The second one - "Plan of the activities related to the project's results achievement"- is linked to Milestone 11 "Availability of NANCY Demonstrators – First Release" in M30. This plan foresees the activities related to the achievements of the Project's results, expected for the 2nd year (M12-M24) and for the 3rd year (M24-M33) respectively, per each of the three NANCY Pillars, and considering the NANCY components that are to be integrated, tested, evaluated and finally validated through Greek in-lab and Italian in-lab testbeds. It is important to highlight that component providers, hardware or software, are required to provide these types of tests:

- Unit tests (in case the code is available);
- Functional tests verifying the intended functionality of their components;

- Bilateral integration tests verifying the interoperability among different components;
- End-to-end integration (system) tests according to specific scenarios that will be defined for the Italian in-lab testbed.

Based on the DoW in the Grant Agreement, the following two figures show, respectively, for each of the three Nancy Pillars, the expected results for the periods M12-M24 and M25-M36:

Table 1: NANCY Expected results M12 – M24

		Year 2											
		M13	M14	M15	M16	M17	M18	M19	M20	M21	M22	M23	M24
GA Projects Results related to WP6													
Pillar I	**[R1] B-RAN architecture**	[70%] NANCY architecture integration and verification by in-lab experiments											
	[R2] Novel trustworthy grant/cell-free cooperative access mechanisms	[60%] required NFs tested in the simulator and optimized											
	[R3] A novel security and privacy toolbox that contains lightweight consensus mechanisms, and decentralized blockchain components	[100%] components validated in in-lab testbeds											
	[R4] Realistic blockchain and attacks models and an experimental validated B-RAN theoretical framework	[100%] B-RAN particularities and security/privacy gaps verified in in-lab testbeds – [100%] In-lab data driven model created – [100%] Theoretical framework verified by in-lab experiments											
	[R5] A novel quantum key distribution mechanisms to boost end-user privacy												
	[R6] Smart pricing policies	[100%] Smart pricing policies integrated											
Pillar II	**[R7] AI-based B-RAN orchestration with slicer instantiator**	[100%] Association and resource allocation required NFs implemented and integrated in NANCY platform											
	[R8] A novel AI virtualiser for underutilized computational & communication resource exploitation	[80%] development – [100%] simulation-based assessment – [50%] in-lab assessment											
	[R9] Novel self-evolving AI model repository												
	[R10] Experimentally driven reinforcement learning optimization of BRAN	[90%] B-RAN in-lab evaluation, optimization, demonstration [80%] Architecture optimized based on in-lab data											
	[R11] Semantic & goal-oriented communication schemes for beyond Shannon excellence	Semantic communications schemes [50%] simulation-based assessment											
	[R12] An explainable AI framework												
Pillar III	**[R13] Next-generation SDN-enabled MEC for autonomous anomaly detection, self-healing and self-recovery**												
	[R14] A computational aware/provision scaling mechanisms and novel battery as well as computational capabilities aware offloading policies	[100%] development and integration, [100%] simulation-based assessment											
	[R15] User-centric caching mechanisms	[100%] development and integration											

Table 2: NANCY Expected results M25 – M36

		Year 3											
		M25	M26	M27	M28	M29	M30	M31	M32	M33	M34	M35	M36
GA Projects Results related to WP6 Gantt													
Pillar I	**[R1] B-RAN architecture**	[100%] NANCY architecture integrated – [100%] NANCY architecture optimized and verified by real-life experiments											
	[R2] Novel trustworthy grant/cell-free cooperative access mechanisms	[100%] required functions integrated. – [100%] required NFs tested in in-lab testbeds and optimized – [100%] required functions demonstrated											
	[R3] A novel security and privacy toolbox that contains lightweight consensus mechanisms, and decentralized blockchain components	[100%] consensus mechanism assessment in in-lab and outdoor demonstrators – [100%] real-life assessment											
	[R4] Realistic blockchain and attacks models and an experimental validated B-RAN theoretical framework	[100%] B-RAN particularities security/privacy gaps verified in real-life testbeds - [100%] Theoretical framework real-life verification											
	[R5] A novel quantum key distribution mechanism to boost end-user privacy	[100%] in-lab and real-life validation, assessment and demonstration											
	[R6] Smart pricing policies	[100%] Smart pricing policies tested in real-life demonstrator											
Pillar II	**[R7] AI-based B-RAN orchestration with slicer instantiator**	[100%] Association and resource allocation NFs tested and assessed in in-lab experiments. - [100%] Association and resource allocation NFs real-life assessment.											
	[R8] A novel AI virtualiser for underutilized computational & communication resource exploitation	[100%] in-lab assessment - [100%] demonstration											
	[R9] Novel self-evolving AI model repository	[100%] functionalities validation											
	[R10] Experimentally driven reinforcement learning optimization of BRAN	[100 %] Architecture optimized based on in-lab data - [100%] Architecture optimized based on real-life data											
	[R11] Semantic & goal-oriented communication schemes for beyond Shannon excellence	Semantic communication schemes [100%] simulation-based assessment - [100%] In-lab demonstration											
	[R12] An explainable AI framework	An explainable AI framework [100%] framework simulation, in-lab and real-life assessment											
Pillar III	**[R13] Next-generation SDN-enabled MEC for autonomous anomaly detection, self-healing and self-recovery**	[100%] mechanism validation											
	[R14] A computational aware/provision scaling mechanisms and novel battery as well as computational capabilities aware offloading policies	[100%] in-lab and real-life validation											
	[R15] User-centric caching mechanisms	[100%] in-lab and real-life validation											

The expected results mentioned above are linked to each one of the two testbeds, Greek and Italian, according to the table below:

Table 3: NANCY Expected results to testbeds mapping

GA Projects Results related to WP6		Greek in-lab testbed	Italian in-lab testbed
Pillar I	**[R1] B-RAN architecture**	×	×
	[R2] Novel trustworthy grant/cell-free cooperative access mechanisms		×
	[R3] A novel security and privacy toolbox that contains lightweight consensus mechanisms, and decentralized blockchain components	x	×

	[R4] Realistic blockchain and attacks models and an experimental validated B-RAN theoretical framework		×
	[R5] A novel quantum key distribution mechanism to boost end-user privacy		x
	[R6] Smart pricing policies	×	
Pillar II	**[R7] AI-based B-RAN orchestration with slicer instantiator**	×	×
	[R8] A novel AI virtualiser for underutilized computational & communication resource exploitation	×	×
	[R9] Novel self-evolving AI model repository	×	×
	[R10] Experimentally driven reinforcement learning optimization of BRAN	×	×
	[R11] Semantic & goal-oriented communication schemes for beyond Shannon excellence		×
	[R12] An explainable AI framework	×	×
Pillar III	**[R13] Next-generation SDN-enabled MEC for autonomous anomaly detection, self-healing and self-recovery**	×	
	[R14] A computational aware/provision scaling mechanisms and novel battery as well as computational capabilities aware offloading policies	×	×
	[R15] User-centric caching mechanisms	×	×

In addition, the relevant NANCY usage scenarios for the two testbeds are represented in the following table:

Table 4: NANCY's Usage scenarios to testbeds mapping

Usage Scenario	Greek in-lab testbed	Italian in-lab testbed
Usage Scenario 1		x
Usage Scenario 2	x	
Usage Scenario 3	(Spanish outdoor demonstrator)	

The above assumptions, together with the plan that controls the development and release of each one of the individual initial architectural components, govern the plan for the second phase. Furthermore, these development and release plans will be outlined in more detail once the architecture is defined, in collaboration with the partner leading each respective development task. In broad outlines, the plan of the second phase is composed of the following steps:

1. Identification of the NANCY components relevant for the Greek in-lab testbed and Italian in-lab testbed, respectively, and related KPIs and Key Value Indicators (KVIs).
2. NANCY components relevant for Greek in-lab testbed and Italian in-lab testbed, respectively, deployment and configuration.
3. Tests execution (automated and/or manual if necessary).
4. Tests report.
5. Availability of NANCY Greek in-lab and Italian in-lab testbeds, respectively, – First release (linked to MS11).
6. Components demonstration and evaluation (measured KPIs).
7. Final validation, against the expected KPIs (final NANCY system performance assessment with data coming from Greek in-lab testbed and Italian in-lab testbed, respectively).

Based on the initial architecture design, the first step has started, and the following architectural components were identified:

- Blockchain_sub1 "Mechanisms for ensuring the security and privacy of the users"

- Blockchain_sub2 "Digital signatures"
- Blockchain_sub3 "Blockchain-based network"
- Blockchain_sub4 "Marketplace"
- Blockchain_sub5 "Deployment of the NANCY Smart Contract"
- Blockchain_sub6 "Digital Contract Creator"
- Anomaly detection,
- AI-based orchestration,
- Task offloading,
- Caching mechanisms,
- PQC signature Blockchain,
- PQC for Secure Communication,
- Self-healing and self-recovery,
- Smart pricing,
- Cell-free access mechanisms
- EXplainable AI (XAI)

The table below shows which of the aforementioned components are pertaining to each of the testbeds[8]:

Table 5: NANCY's Architectural components to testbeds mapping

Initial architectural component	Greek in-lab testbed			Italian in-lab testbed		
	Pillar I	**Pillar II**	**Pillar III**	**Pillar I**	**Pillar II**	**Pillar III**
Blockchain_sub1 "Mechanisms for ensuring the security and privacy of the users"	O[9]	O	O	O	O	O
Blockchain_sub2 "Digital signatures"	O	O	O	X	O	O
Blockchain_sub3 "Blockchain-based network"	X[10]	X	X	X	X	X
Blockchain_sub4 "Marketplace"	X	X	X	X	X	X
Blockchain_sub5 "Deployment of the NANCY Smart Contract"	X	X	X	X	X	X
Blockchain_sub6 "Digital Contract Creator"	X	X	X	X	X	X
Anomaly detection	X	X	X	X	X	X
AI-based orchestration	O	X	-	O	X	-
Task offloading	X	X	X	X	X	X
Caching mechanisms	X	X	X	X	X	X
PQC signature Blockchain	-	-	-	X	X	X
PQC for Secure Communication[11]	-	-	-	-	-	-
Self-healing and self-recovery	X	X	X	-	-	-
Smart pricing	X	X	X	-	-	-
Cell-free access mechanisms[12]	-	-	-	-	-	-
EXplainable AI (XAI)	X	X	X	-	-	-

[8] The division of the components participating in the testbeds into three pillars (three columns for each testbed) is because some results are related to different architectural components.
[9] i.e., Optional
[10] i.e., Mandatory
[11] PQC for Secure Communication will be demonstrated at Italian massive-IoT Demonstrator.
[12] Cell-free access mechanisms will be instantiated at the Spanish testbed.

4. Evaluation Methodology and outcomes

The two previously outlined testbeds will produce data tailored to their respective usage scenarios. In particular, their primary objective is to generate datasets to provide adequate experimental data for the development of the B-RAN and attack models for the NANCY framework. In this regard, two dataset versions will be generated in the context of the Greek in-lab testbed, namely D6.5 and D6.7 - "Greek in-lab testbed dataset 1/2", respectively. The experimental data will be incorporated into WP2, as illustrated in Figure 14: Interaction with other WPs, in order to derive and evaluate the theoretical framework. They will also contribute significantly to the training of the AI models developed in WP4. These datasets are obtained from network traffic collected at various points along the testbed topology. In the same direction, the experimental data 1 and 2 of the Italian testbed, namely D6.6 and D6.8 – "Italian in-lab testbed dataset 1/2", respectively, are crucial in the NANCY project's mission to further develop and optimize the capabilities of B-RAN networks and related technologies in the context of Usage Scenario 1: "Fronthaul network of fixed topology – Direct Connectivity & Coordinated Multi Point (CoMP)". These datasets will not only assist in the development of B-RAN and attack models but also support WP2's performance evaluation of B-RAN through modelling and testbed results.

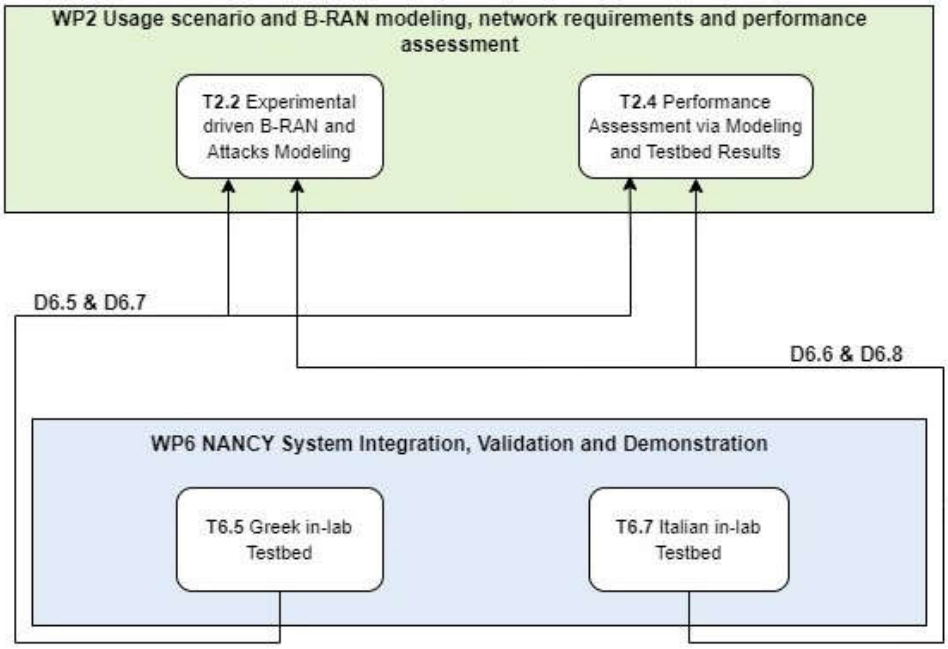

Figure 14: Interaction with other WPs

4.1. Greek in-lab testbed dataset 1 & 2

The Greek in-lab testbed is focused on assessing and validating the developments of NANCY with respect to Usage Scenario 2: Advanced Coverage Expansion. In this direction, two dataset versions will be generated, namely D6.5 and D6.7 – "Greek in-lab testbed dataset 1/2". The datasets will consist of network traffic that will be captured from three points of the testbed topology (see Figure 7: Greek in-lab testbed topology), specifically from the BS, the intermediate node, and the UEs. The generated datasets will be used for training the AI models that will be developed in the context of WP4. Some indicative measurements that will be recorded include the following:

- Peak and average throughput

- Packet loss rate
- Radio resources scheduled to the UE
- Signal-to-noise-ratio (SNR) values
- Received signal strength indicator (RSSI)
- Computing resource utilization

4.2. Italian in-lab testbed dataset 1 & 2

It is important to start by reminding that the goal of Italian in-lab testbed is to test and validate the technology developed by NANCY in a limited laboratory environment. In this environment, the network conditions are measured and controlled to produce a set of data relevant to the Usage Scenario 1: "Fronthaul network of fixed topology – Direct Connectivity & Coordinated Multi Point (CoMP) connectivity". Two dataset versions will be generated, namely D6.6 and D6.8 – "Italian in-lab testbed dataset 1/2".

Some of the following measurements will be carried out in the Italian in-lab testbed in order to produce experimental data to test and validate the technology developed by NANCY:

- General parameters, to better characterize the related measured data: Timestamp of all measurements and procedures, UE's position, BS's position, Area map, Antenna types, Antenna characteristics
- E2E Service Latency
- Peak Data Rate
- Average Data Rate
- Bandwidth per terminal
- User Density (1 – for Dataset 1)
- Peak SNR
- Average SNR
- Peak RSS
- Average RSS Radio Signal strength
- Packet Loss Rate
- Edge computational resource usage

The derived datasets enable exploiting prior knowledge of the system, based on mathematical models, as the initialization point from which AI methods start interacting with the environment for further system optimization. The experimental data will be used by AI methods to analyse e.g., the topology, channel assignment, and other parameters of the current wireless network and to define the model of the initial network status, considering the specific characteristics relevant for the usage scenario 1.

5. Conclusion

D6.4 – “In-lab testbeds Definition” demonstrates the preliminary steps for establishing and defining the Greek and Italian in-lab testbeds. These testbeds serve an important role in the B-RAN modelling and in validating the theoretical framework described in WP2 in the context of real-world usage scenarios. Moreover, the deliverable aims to present plans and specifications for the anticipated activities in each of the testbeds described above, highlighting their fundamental contribution to the overall success of the project. In addition, the present document provides an extensive overview of all the associated components and their respective specifications that will compose each testbed. Finally, D6.4 - “'In-lab testbeds Definition” will initiate the process of collecting experimental data during these testbeds, which will be beneficial in obtaining a greater awareness of the overall NANCY system and facilitating further optimization.

References

[1] L. Giupponi and F. Wilhelmi, "Blockchain-Enabled Network Sharing for O-RAN in 5G and Beyond," IEEE Network, vol. 36, no. 4, pp. 218-225, July/August 2022.

[2] M. A. Khan, E. Baccour, Z. Chkirbene, A. Erbad, R. Hamila, M. Hamdi, and M. Gabbouj., "A Survey on Mobile Edge Computing for Video Streaming: Opportunities and Challenges," IEEE Access, vol. 10, pp. 120514-120550, 2022.

Appendix 1: Open5GS

Open5GS is an open-source implementation of the 5G core and evolved packet core (EPC) network and aims to simplify the deployment of 5G using general-purpose hardware. The project covers key components of the 5G and EPC, including access and mobility function (AMF), user plane function (UPF), and session management function (SMF), serving gateway (SGW), mobility management entity (MME), and packet data network gateway (PGW). Open5GS aims to make 5G technology more accessible by providing an affordable and adaptable option compared to traditional hardware-centric core network systems. Open5GS is compliant with the 3GPP specifications and has an active research and development community. Open5GS has a flexible design, thereby it is able to adapt to different requirements, ranging from lab testbeds to large commercial deployments.

Appendix 2: OpenAirInterface

The OpenAirInterface-5G Core Network (OAI-5G CN) component is an open-source core network implementation that is compliant with the 3GPP specifications. OAI-5G CN aims to offer a flexible 5G core solution that can adapt to various scenarios and needs, such as laboratory testbeds or large-scale deployments. All components are deployed as containers in order to facilitate the deployment process and the integration of new functionalities Additionally, this deployment process enables the utilization of orchestration solutions such as Kubernetes.

Additionally, OpenAir Interface 5G (OAI-5G) is an implementation of the 5G RAN software stack that includes distributed unit (DU) and centralized unit (CU) functionalities. Also, it supports backward compatibility with non-standalone (NSA) infrastructure deployments. Furthermore, OAI-5G includes a radio channel simulation tool for facilitating the development and validation of higher-level applications, acceleration and offloading of the L1 layer, and further enhancements to the CU and DU disaggregated functionalities.

Appendix 3: srsRAN

srsRAN is an open-source software radio suite, developed by Software Radio System, that enables the deployment of 4G and 5G base stations (i.e., eNodeB (eNB) and gNodeB (gNB), respectively). srsRAN supports the 3GPP Release 15 which enables the splitting of a gNB into the Radio Unit (RU), Distributed Unit (DU), and Centralized Unit (CU), adhering to the O-RAN specifications. This release enables the deployment of 8 functional splits, that specify how RAN is split into RU, DU, and CU. Specifically, the DU and CU communicate through the F1 interface, while a gNB communicates with other gNBs through the Xn interface. Finally, the RAN communicates with the Core through the NG interface.

Table 6 summarizes the requirements and supported features of srsRAN. It is worth noting, that srsRAN supports the whole Frequency Range 1 (FR1), i.e., the sub-6GHz spectrum, while a Multiple Input-Multiple Output (MIMO) configuration of up to 4x4 antenna elements can be used. Furthermore, five types of bandwidths with two types of sub-carrier spacing can be utilized. Finally, three types of RF front-end devices are supported, namely the Ettus Research USRPs, Nuand BladeRF, and Lime Microsystems LimeSDR.

Table 6: Summary of srsRAN Features

srsRAN Features	
Hardware Requirements	x86-64 PC with at least 4 cores
Programming Language	C/C++

Operating System	Linux-based OS
Frequencies	Sub-6GHz Bands (FR1)
Bandwidth	10, 20, 40, 80, 100 MHz
Antenna Configuration	Up to 4x4 MIMO
Multiplexing Mode	TDD/FDD
Sub-carrier Spacing	15, 30 KHz
Supported RF Front-end	USRP, BladeRF, LimeSDR
License	GNU Affero General Public License v3

An instance of the srsRAN gNB software is depicted in Figure 15. In more detail, the screenshot depicts the initialization of the connection between the gNB and the USRP, as well as the connection with the near real-time RIC. Additionally, statistics about the downlink and uplink channels are shown.

```
ithaca@usrpbox:~$ sudo gnb -c ~/Desktop/configs/gnb_usrp.yaml
Lower PHY in quad executor mode.

--== srsRAN gNB (commit 1afd7240f) ==--

Connecting to AMF on 127.0.0.5:38412
Available radio types: uhd and zmq.
[INFO] [UHD] linux; GNU C++ version 11.4.0; Boost_107400; UHD_4.4.0.0-265-ga2a04e31
[INFO] [LOGGING] Fastpath logging disabled at runtime.
Making USRP object with args 'type=x300,num_recv_frames=64,num_send_frames=64,master_clock_rate=184.32e6,
send_frame_size=8000,recv_frame_size=8000'
[INFO] [X300] X300 initialization sequence...
[INFO] [X300] Maximum frame size: 8000 bytes.
[INFO] [X300] Radio 1x clock: 184.32 MHz
[WARNING] [0/Radio#0] Attempting to set tick rate to 0. Skipping.
Connecting to NearRT-RIC on 127.0.0.1:36421
Cell pci=1, bw=10 MHz, dl_arfcn=368500 (n3), dl_freq=1842.5 MHz, dl_ssb_arfcn=368410, ul_freq=1747.5 MHz

==== gNodeB started ===
Type <t> to view trace
          ----------------DL----------------|------------------UL----------------------
 pci rnti  cqi  ri  mcs  brate   ok  nok  (%) | pusch  mcs  brate   ok  nok  (%)    bsr
   1 4601   14   1   26   2.2k    4    0   0% |  16.2   20    23k    7    0   0%    0.0
   1 4601   14   1    0      0    0    0   0% |   n/a    0      0    0    0   0%    0.0
   1 4601   14   1    0      0    0    0   0% |   n/a    0      0    0    0   0%    0.0
   1 4601   14   1    0      0    0    0   0% |   n/a    0      0    0    0   0%    0.0
   1 4601   14   1    0      0    0    0   0% |   n/a    0      0    0    0   0%    0.0
   1 4601   14   1   26    552    1    0   0% |  17.6   19   4.4k    1    0   0%    0.0
   1 4601   14   1   26   2.2k    4    0   0% |  16.4   20    22k    5    0   0%    0.0
   1 4601   15   1   27   2.9k    5    0   0% |  16.1   20    22k    5    0   0%    0.0
   1 4601   15   1   26   3.4k    6    0   0% |  15.9   20    26k    6    0   0%    0.0
   1 4601   15   1   27   5.2k    9    0   0% |  16.5   20    44k   11    0   0%    0.0
   1 4601   14   1   26   2.2k    4    0   0% |  16.4   20    13k    3    0   0%    0.0

          ----------------DL----------------|------------------UL----------------------
 pci rnti  cqi  ri  mcs  brate   ok  nok  (%) | pusch  mcs  brate   ok  nok  (%)    bsr
   1 4601   14   1   26   1.1k    2    0   0% |  15.4   19   8.7k    2    0   0%    0.0
   1 4601   14   1   26   3.3k    6    0   0% |  15.6   19    32k    7    0   0%    0.0
   1 4601   15   1   27   4.0k    7    0   0% |  15.5   19    41k    9    0   0%    0.0
   1 4601   14   1   26   5.1k    9    0   0% |  15.6   19    49k   13    0   0%    0.0
   1 4601   14   1   26   3.9k    7    0   0% |  15.7   19    56k   10    0   0%    0.0
   1 4601   14   1   26   3.3k    6    0   0% |  15.0   18    26k    6    0   0%    0.0
   1 4601   14   1   26   2.8k    5    0   0% |  15.5   19    22k    5    0   0%    0.0
   1 4601   14   1   26   3.9k    7    0   0% |  15.6   19    39k    9    0   0%    0.0
   1 4601   14   1   26   3.9k    7    0   0% |  15.1   19    58k   11    5  31%    0.0
   1 4601   14   1   26   3.3k    6    0   0% |  15.9   19    35k    8    0   0%    0.0
   1 4601   14   1   26   2.2k    4    0   0% |  15.7   19    22k    5    0   0%    0.0
```

Figure 15: gNB Initialization and UE Association

Similarly, Figure 16 depicts the connection initialization between the gNB and the near real-time RIC, while Figure 17 depicts the AMF log, indicating that a UE has been connected to the gNB.

```
ithaca@usrpbox:~$ ./flexric/build/examples/ric/nearRT-RIC
Setting the config -c file to /usr/local/etc/flexric/flexric.conf
Setting path -p for the shared libraries to /usr/local/lib/flexric/
[NEAR-RIC]: nearRT-RIC IP Address = 127.0.0.1, PORT = 36421
[NEAR-RIC]: Initializing
[NEAR-RIC]: Loading SM ID = 143 with def = RLC_STATS_V0
[NEAR-RIC]: Loading SM ID = 147 with def = ORAN-E2SM-KPM
[NEAR-RIC]: Loading SM ID = 142 with def = MAC_STATS_V0
[NEAR-RIC]: Loading SM ID = 148 with def = GTP_STATS_V0
[NEAR-RIC]: Loading SM ID = 144 with def = PDCP_STATS_V0
[NEAR-RIC]: Loading SM ID = 146 with def = TC_STATS_V0
[NEAR-RIC]: Loading SM ID = 145 with def = SLICE_STATS_V0
[iApp]: Initializing ...
[iApp]: nearRT-RIC IP Address = 127.0.0.1, PORT = 36422
fd created with 6
Received message with id = 411, port = 204
[E2AP] Received SETUP-REQUEST from PLMN   1. 1 Node ID 411 RAN type ngran_gNB
[NEAR-RIC]: Accepting RAN function ID 147 with def = `0ORAN-E2SM-KPM
[NEAR-RIC]: Accepting interfaceType 0
```

Figure 16: RIC initialization and connection with the gNB

```
ithaca@usrpbox:~$ sudo tail -f /var/log/open5gs/amf.log
[sudo] password for ithaca:
11/09 17:43:57.020: [amf] INFO: gNB-N2 accepted[127.0.0.1]:57965 in ng-path module (../src/amf/ngap-sctp.
c:113)
11/09 17:43:57.020: [amf] INFO: gNB-N2 accepted[127.0.0.1] in master_sm module (../src/amf/amf-sm.c:741)
11/09 17:43:57.020: [amf] INFO: [Added] Number of gNBs is now 1 (../src/amf/context.c:1185)
11/09 17:43:57.020: [amf] INFO: gNB-N2[127.0.0.1] max_num_of_ostreams : 30 (../src/amf/amf-sm.c:780)
11/09 17:44:02.855: [amf] INFO: InitialUEMessage (../src/amf/ngap-handler.c:401)
11/09 17:44:02.855: [amf] INFO: [Added] Number of gNB-UEs is now 1 (../src/amf/context.c:2523)
11/09 17:44:02.855: [amf] INFO:     RAN_UE_NGAP_ID[0] AMF_UE_NGAP_ID[7] TAC[7] CellID[0x19b0] (../src/amf
/ngap-handler.c:562)
11/09 17:44:02.855: [amf] INFO: [suci-0-001-01-0-0-0-0000048163] Known UE by 5G-S_TMSI[AMF_ID:0x20040,M_T
MSI:0xc0000658] (../src/amf/context.c:1850)
11/09 17:44:02.855: [gmm] INFO: Service request (../src/amf/gmm-sm.c:1171)
11/09 17:44:02.855: [gmm] INFO: [suci-0-001-01-0-0-0-0000048163]    5G-S_GUTI[AMF_ID:0x20040,M_TMSI:0xc00
00658] (../src/amf/gmm-handler.c:658)
11/09 17:44:03.016: [amf] INFO: [imsi-001010000048163:1:11][0:0:NULL] /nsmf-pdusession/v1/sm-contexts/{sm
ContextRef}/modify (../src/amf/nsmf-handler.c:837)
```

Figure 17: AMF log indicating the successful connection between the gNB and a UE

Appendix 4: SD-RAN

The SD-RAN project is developed by Open Networking Foundation (ONF) in the context open radio access network (RAN) ecosystem. The project is focused on developing an open source, cloud-native version of the O-RAN near real-time radio intelligent controller (near-RT RIC). In parallel, open APIs to host RAN applications, known as xApps, are designed to manage RAN operations. To support this, the ONF is rolling out a software development kit (SDK) to simplify the creation of new xApps. These xApps can work with both standardized E2 Service Models (E2SMs) and custom service models from the SD-RAN community. The foundation of this RIC is the Open Networking Operating System (ONOS) controller, which includes a set of microservices supporting various functionalities such as xApp subscriptions and user information to data storage and operator requirements.

The SD-RAN platform implements the O-RAN specifications focusing on virtualization and software-driven control of the O-RAN components leveraging the latest orchestration and software delivery tools. Leveraging the micro-services paradigm SD-RAN offers a disaggregated environment operating on well-known orchestrators such as Kubernetes. At its core SD-RAN makes use of the micro-ONOS controller, the next generation of the ONOS platform that is cloud native and supports the latest data plane technologies and communication protocols, to manage and control the RAN whereas the micro-services environment enables flexibility in terms of CU/DU solutions placement of software components on commercial off-the-shelf (COTS) and application-specific targets.

Appendix 5: FlexRIC

FlexRIC aims to facilitate the development of customized RAN controllers in order to address the needs of specific usage scenarios. It is composed of two main components, namely the RAN agent and the real-time controller, that extend the capabilities of a BS by integrating RAN functionality (e.g., monitoring and control). FlexRIC has a built-in service model for monitoring and slicing, which is highly customizable, making it well-suited for a wide range of use cases. Also, the application protocol and service model encoding- and decoding-agnostic. Consequently, FlexRIC can be integrated into different network scenarios and accommodate different encoding and decoding standards.

Appendix 6: USRP X310 and UBX 160 USRP Daughterboard

The Ettus Research USRP X310 is a high-performance, scalable software-defined radio (SDR) platform for designing and deploying next-generation wireless communications systems. The hardware architecture combines two extended-bandwidth daughterboard slots covering DC – 6 GHz with up to 160 MHz of baseband bandwidth, multiple high-speed interface options (PCIe, dual 10 GigE, dual 1 GigE), and a large user-programmable Kintex-7 FPGA in a convenient desktop or rack-mountable half-wide 1U form factor.

Figure 18: USRP X310

The main features are the following:

- Two wideband RF daughterboard slots
  - Up 160MHz bandwidth per channel
  - Selection covers DC to 6 GHz
- Large, customizable Kintex-7 FPGA
  - USRP X300 - XC7K325T
  - USRP X310 – XC7K410T
- UHD architecture provides compatibility:
  - GNURadio
  - C++ API/Python
  - Other third-party frameworks & applications
- Multiple high-speed interfaces
  - Dual SFP(+) ports for 1/10 Gigabit Ethernet
  - PCIe x4
- Flexible clocking architecture
  - Configurable sample clock
  - Optional GPS-disciplined OCXO
  - Coherent operation with 10 MHz/1 PPS
- Compact and rugged half-wide 1U form factor

In the Italian in-lab testbed, the USRP X310 is equipped with nr. 2 UBX 160 USRP Daughterboard (10 MHz - 6 GHz, 160 MHz BW) for the radio part. The UBX 160 daughterboard is a full-duplex wideband transceiver that covers frequencies from 10 MHz to 6 GHz with up to 160 MHz* of instantaneous bandwidth. Coherent and phase-aligned operation across multiple UBX daughterboards enables users to explore MIMO and direction-finding applications.

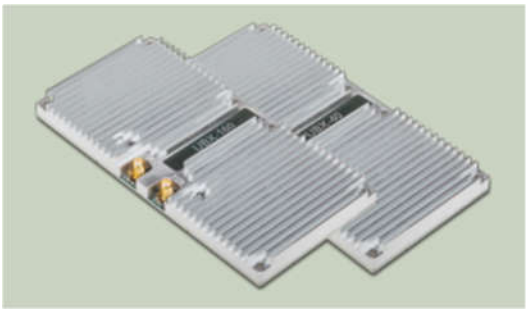

Figure 19: UBX 160 USRP Daughterboard

The table below reports the main characteristics of UBX 160 USRP Daughterboard:

Table 7: Characteristics of UBX 160 USRP Daughterboard

UBX 160 USRP Daughterboard	
Wide RF Coverage	10 MHz to 6GHz
Wide bandwidth	Up to 160 MHz
USRP Compatibility	X Series and N Series
Full-Duplex Operation RF Shielding Coherent and phase-aligned operation	

Appendix 7: Ettus Research USRP B210

The Ettus Research USRP B210 is a single-board software defined radio (SDR) device that supports frequencies from 70 MHz to 6 GHz and is specifically designed for affordable SDR experimentation. USRP B210 integrates a RF frontend based on the Analog Devices AD9361 transceiver, supporting up to 56 MHz of real-time RF bandwidth, as well as SISO and MIMO capabilities. Furthermore, a Spartan-6 XC6SLX150 FPGA is employed to control the transceiver and carry out signal processing functionalities. A USB 3.0 is used as a physical interface for connecting B210 to a host computer, offering a sample throughput of up to 61.44 million samples/second (MS/s). Finally, the USRP hardware driver (UHD) is used for facilitating the development of SDR-based applications. Figure 20 depicts the USRP B210, while Table 8 summarizes its specifications.

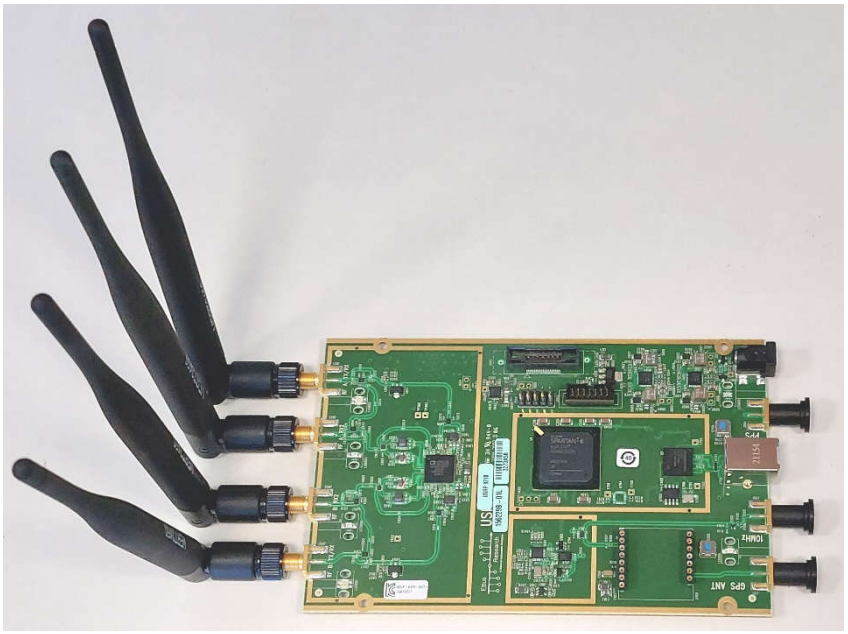

Figure 20: Ettus Research USRP B210

Table 8: Ettus Research USRP B210 Specifications

Ettus Research USRP B210	
Supported Frequencies	70 MHz to 6 GHz
Antenna Configuration	2x2 Half/Full Duplex
Transceiver	Analog Devices AD9361
Processor	Spartan-6 XC6SLX150
Bandwidth	Up to 56 MHz in 1x1 SISO Configuration Up to 30.72 MHz in 2x2 MIMO Configuration

Appendix 8: Texas Instruments SK-AM69

The SK-AM69x Texas Instruments board is a powerful embedded solution designed to excel in edge computing applications. This board features edge AI, vision, analytics and general-purpose processors, including:

- Up to eight 64-bit Arm Cortex-A72 microprocessors
- An image signal processor (ISP) supporting up to 1440MP/s
- An AI vision assist accelerator able to carry-out 32 tera-operations-per-second (TOPS)

The board additionally features a substantial amount of RAM and storage, enabling it to store and manipulate large datasets and execute resource-demanding applications in a seamless way. More specifically, it features 4 DRAMs LPDDR4-4266 providing a total memory capacity of 32GBs, 32GB eMMC and 512MB Non-Volatile Flash.

Figure 21: SK-AM69 board

The table below demonstrates the main features of the SK-AM69 board:

Table 9: Features of the SK-AM69 board

Texas Instruments AM69x Starter Kit	
Processor	8x 64-bit ARM Cortex-A72 ISP 1440MP/s AI accelerator 32 TOPS
Memory	4x 8GByte LPDDR4 DRAM (2133 MHz) 512 Mb Non-Volatile Flash, Octal-SPI NOR 32GB eMMC, version 5.1 compliant Multimedia Card (MMC)/Secure Digital Card (Micro SD) Cage, UHS-I
Optimized Power Management solution	Dynamic Voltage Scaling Multiple Clock and Power Domains
USB	USB3.1 (Gen1) Hub to 3x Type A (Host) USB3.1 (Gen1) Type C (DFP modes) USB2.0 Micro B (for Quad UART-over-USB Transceiver)
Display	VESA Display Port (v1.4), supports 4K UHD with MST support DVI (v1.0) via HDMI Type A, supports 1080p
Wired Network	Gigabit Ethernet (RJ45 Connector) 4x CAN-FD Headers (1x3)
Camera Interfaces	2x 22-Pin Flex Cable Interface (CSI-4L) 2x 40-pin High Speed Connector (dual CSI-4L, I2C, GPIO, and so forth)
Expansion/ Add-on	M.2 Key M Interface (PCIe/Gen3 x 2 Lane) M.2 Key E Interface (PCIe/Gen3 x 1 Lane) Standard x8 PCIe Interface (Gen3 x 4 Lane) 60-pin ENET expansion header SGMII Interface 40-pin Header (2x20) (I2C, SPI, UART, I2S, GPIO, PWM, and so forth) Fan Header (12 V)
User control/ Indication	Pushbuttons (Reset, Power/User Defined) LEDs (Power, User Defined, Serial Port) User Configuration (Boot Mode) On board Emulator Support (XDS110) with optional external support (20-pin Header)

In the Italian in-lab testbed, the SK-AM69x will be integrated as a powerful MEC edge server, able to perform tasks that rely on fast, efficient, and reliable data processing. Making possible to handle complex algorithms and data-intensive applications, it is considered an ideal choice for a variety of edge computing tasks.

Appendix 9: Google Pixel7 Android 5G, Moto G100

Google Pixel7 is an Android phone designed, developed, and marketed by Google as part of the Google Pixel product line.

Figure 22: Google Pixel7 Android 5G

It is powered by the second-generation Google Tensor system-on-chip (SoC). It has a 6.3 in (160.5 mm) FHD+ 1080p OLED display at 416 ppi with a 2400 × 1080-pixel resolution and a 20:9 aspect ratio and has a 90 Hz refresh rate.

The table below reports the main characteristics of the smartphone:

Table 10: Characteristics of Google Pixel7 smartphone

Google Pixel7 Android 5G	
Operating system	Android 13
Display	Full-screen 6.3-inch (160.5 mm) display 20:9 aspect ratio FHD+ (1080 x 2400) OLED at 416 PPI Smooth Display (up to 90 HZ) Always-on display At a Glance Now Playing
Dimensions and Weight	Dimensions: 6.1 height x 2.9 width x 0.3 depth (inches) 155.6 height x 73.2 width x 8.7 depth (mm) Weight: 197 g 6.9 oz
Battery	Beyond 24-hour battery life Up to 72-hour battery life with Extreme Battery Saver Minimum 4270 mAh

	Typical 4355 mAh
Memory and Storage	Memory: 8 GB LPDDR5 RAM Storage: 128 GB / 256 GB UFS 3.1 storage
Processors	Google Tensor G2 Titan M2TM security coprocessor
Video	Rear Camera: 4K video recording at 30 FPS, 60 FPS 1080p video recording at 30 FPS, 60 FPS 10-bit HDR video Front Camera: 4K video recording at 30 FPS, 60 FPS 10-bit HDR video Cinematic Blur Cinematic Pan Slo-mo video support up to 240 FPS 4K timelapse with stabilization Astrophotography timelapse Optical image stabilization Fused video stabilization 4K Cinematic Pan video stabilization 4K Locked video stabilization 1080p Active video stabilization Digital zoom up to 7x12 Video formats: HEVC (H.265) and AVC (H.264) Audio: Stereo recording Speech enhancement Wind noise reduction Audio zoom
Buttons and Ports	USB Type-C® 3.2 Gen 2 Power button Volume controls
SIMs	Dual SIM (Single Nano SIM and eSIM13)
Wireless and Location	US (PR), CA, UK, EU, AU: Wi-Fi 6E (802.11ax) with 2.4GHz+5GHz+6GHz, HE160, MIMO TW, JP, SG, IN: Wi-Fi 6 (802.11ax) with 2.4GHz+5GHz, HE160, MIMO Bluetooth® v5.2 with dual antennas for enhanced quality and connection NFC Google Cast Location **US**: Dual Band GNSS GPS, GLONASS, Galileo, QZSS **IN**: Dual Band GNSS GPS, GLONASS, Galileo, QZSS, BeiDou,

	NavIC **Rest of the world**: Dual Band GNSS GPS, GLONASS, Galileo, QZSS, BeiDou
Networks	[5G Sub 6GHz] Model GVU6C • GSM/EDGE: Quad-band (850, 900, 1800, 1900 MHz) • UMTS/HSPA+/HSDPA: Bands 1,2,4,5,6,8,19 • LTE: Bands B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/29/30/32/38/39/40/41/46/48/66/71 • 5G Sub-6: Bands n1/2/3/5/7/8/12/14/20/25/28/30/38/40/41/48/66/71/75/76/77/78 • eSIM [5G mmWave + Sub 6GHz] Model GQML316 • GSM/EDGE: Quad-band (850, 900, 1800, 1900 MHz) • UMTS/HSPA+/HSDPA: Bands 1,2,4,5,6,8,19 • LTE: Bands B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/29/30/38/40/41/46/48/66/71 • 5G Sub-615: Bands n1/2/3/5/7/8/12/14/20/25/28/30/38/40/41/48/66/71/77/78 • 5G mmWave: Bands n260/n261 • eSIM

MotoG 100 is an Android smartphone that belongs to the Moto G family developed by Motorola Mobility, a subsidiary of Lenovo.

Figure 23: MotoG 100

It is powered by 3.2 GHz Octa-core processor, and it comes with 8GB of RAM. The Motorola Moto G100 packs 128GB of internal storage that can be expanded via microSDXC (uses shared SIM slot). The Motorola Moto G100 runs Android 11 and is powered by a 5000mAh non-removable battery.

The table below reports the main characteristics of the smartphone:

Table 11: MotoG 100 smartphone characteristics

MotoG 100	
Operating system	Android™ 11
Display	Display Size - 6.7" display Resolution - FHD+ (2520 x 1080) Screen to Body Ratio - 85% Display Technology - LCD, 90Hz refresh rate, DCI-P3 colour space, HDR10 Aspect Ratio - 21:9 CinemaVision
Dimensions and Weight	Dimensions: 168.38 x 73.97 x 9.69m Weight: 207g
Battery	Battery Size - 5000mAh Battery Life - Over 40 hours of battery life Charging - TurboPower™ 20
Memory and Storage	Memory: 8GB LPDDR5 RAM Internal Storage: 128GB UFS 3.1 built-in* with Turbo Write and Host-Aware Performance Booster, Up to 1TB microSD card expandable
Processors	Qualcomm® Snapdragon™ 870 5G Mobile Platform Adreno™ 650 GPU
Video	Rear Camera Video Capture: Rear main camera: 6K UHD (30fps) | 4K UHD (30/60fps) | FHD (60/30fps) | Slow motion FHD (120fps) or HD (240fps) Rear ultra-wide angle camera: 4K UHD (30fps) | FHD (30/60fps) Front Camera Video Capture: Main selfie camera: FHD (30fps) Ultra-wide angle selfie camera: FHD (30fps)
Ports	3.5mm headset jack & Type-C port (USB 3.1 compatible) with DisplayPort
SIMs	Hybrid Dual SIM (2 Nano SIMs, 5G + 4G, or 1 Nano SIM + 1 microSD)
Connectivity and Location	Networks - 5G: NR sub-6GHz | 4G: LTE (UL Cat 13 / DL Cat 18) | 3G: UMTS / HSPA+ | 2G: GSM / EDGE Bands - 5G: sub-6GHz band n1/n3/n5/n7/n8/n28/n38/n41/n66/n77/n78 | 4G: LTE band 1/2/3/4/5/7/8/12/13/17/20/26/28/32/34/38/39/40/41/42/43/66 | 3G: UMTS band 1/2/4/5/8 | 2G: CDMA band 0/1 | 2G: GSM band 2/3/5/8 Bluetooth Technology - Bluetooth® 5.1 NFC - Yes Wi-Fi - Wi-Fi 802.11 a/b/g/n/ac/ax - 2.4 GHz | 5 GHz - WiFi hotspot - WiFi 6 Location Services - GPS, AGPS, LTEPP, SUPL, GLONASS, Galileo

Appendix 10: Intel® NUC

The NUC "RNUC12WSKI70000 Intel Next Unit of Computing 12 Pro Kit - NUC12WSKI7 - Slim Chassis - Core i7 1260P" is a small form factor device or compute element that delivers a full edge device experience. A NUC contains everything a standard PC does: processor, memory, SSD, LAN or Wi-Fi, and support for integrated and discrete graphics options. The kit includes the processor, motherboard, and chassis but allows you to add your choice of memory, storage, and peripherals to create your solution for the specific situation.

Figure 24: Intel Next Unit of Computing (NUC) 12 Pro Kit - NUC12WSKI7 in the Italian testbed

The table below reports the main characteristics of the NUC:

Table 12: Characteristics of NUC

Intel NUC 12 Pro Kit - NUC12WSKI7	
Product collection	Intel® NUC Mini PC with 12th Generation Intel® Core™ Processors
Processor included	Intel® Core™ i7-1260P Processor (18M Cache, up to 4.70 GHz)
Supported Operating Systems	Windows 11 Home*, Windows 11 Pro*, Windows 10 Home*, Windows 10 IoT Enterprise*, Windows 10 Pro*, Red Hat Linux*, Ubuntu 20.04 LTS*
CPU specifications	Total Cores 12 Total Threads 16 Max Turbo Frequency 4.70 GHz
I/O specifications	Graphics Output 2x HDMI 2.1 TMDS Compatible Nr. of Displays Supported: 2 Nr. of USB Ports: 4 USB ConfigurationFront: 2x USB 3.2 Rear: 1x USB 3.2, 1x USB 2.0 Internal: 1x USB 3.2 on m.2 22x42 (pins), 2x USB 2.0 (headers) Serial Port via Internal Header: No Audio (back channel + front channel): Front panel: 3.5mm headphone/mic jack

	Integrated LAN (i.e., the presence of an integrated Intel Ethernet MAC or presence of the LAN ports built into the system board): Intel® Ethernet Controller i225-V Wireless Included: Intel® Wi-Fi 6E AX211 (Gig+) Bluetooth Version: 5.3 M.2 Card Slot (wireless), i.e., presence of an M.2 slot that's keyed for wireless expansion cards: 22x30 (E) Additional Headers (i.e., presence of additional interfaces such as NFC, auxiliary power, and others): Front panel (PWR, RST, 5V, 5Vsby, 3.3Vsby); Internal 2x2 power connector
Expansion options	PCI Express Revision: Gen 4 (m.2 22x80 slot); Gen 3 (otherwise) (N.B. PCI Express Revision is the supported version of the PCI Express standard. Peripheral Component Interconnect Express (or PCIe) is a high-speed serial computer expansion bus standard for attaching hardware devices to a computer. The different PCI Express versions support different data rates.) PCI Express (PCIe) Configurations: PCIe x4 Gen 4: M.2 22x80 (key M) PCIe x1 Gen 3: M.2 22x42 (key B) PCIe x1: M.2 22x30 (key E)
Thermal Design Power (TDP)	35 W
DC Input Voltage Supported	12-20 VDC
Chassis dimensions	117 x 112 x 37 [mm] (LxWxH)
Security & Reliability	- Intel® Platform Trust Technology (Intel® PTT is a platform functionality for credential storage and key management used by Windows 8* and Windows® 10.) - Intel® Management Engine Firmware (Intel® ME FW uses built-in platform capabilities and management and security applications to remotely manage networked computing assets out-of-band.) - Intel® AES New Instructions (Intel® AES-NI are a set of instructions that enable fast and secure data encryption and decryption. AES-NI are valuable for a wide range of cryptographic applications, for example: applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption.)
Board Form Factor	UCFF (4" x 4")

Appendix 11: Quectel RM520N-GL 5G Module with USB Dongle

Quectel RM520N-GL is a module that equips IoT devices with 5G connectivity. It is designed in an M.2 form factor, making it ideal for being integrated into IoT applications. Moreover, the module is based on the 3GPP Release 16 specifications, supporting both standalone (SA) and non-standalone (NSA) 5Gx modes. It supports the sub-6 GHz frequencies, while the maximum rates are 2.4 Gbps downlink (DL) and 900 Mbps uplink (UL) and 3.4 Gbps DL and 550 Mbps UL, respectively for 5G-SA and 5G-NSA. The module is installed in Waveshare's Dongle, which enables the connection with desktop or laptop devices through a USB3 port. The Dongle and the antennas in a 2x2 MIMO configuration are depicted in Figure 25.

Figure 25: USB Dongle with Quectel 5G Module

In addition, Table 13: Quectel RM520-GL 5G Module Features summarizes the 5G module's capabilities.

Table 13: Quectel RM520-GL 5G Module Features

Quectel RM520N-GL 5G Module	
Frequency Bands	Sub-6G (5G-SA & 5G-NSA)
Multiplexing Mode	TDD and FDD
Data rates	2.4 Gbps DL / 900 Mbps UL in 5G-SA mode 3.4 Gbps DL / 550 Mbps UL in 5G-NSA mode
Software Compatibility	Windows/Linux/Android Operating Systems

Hardware Information	SIM card 1.8V/3.0V Antenna connector:4x/ 6x IPEX-4 connector

Appendix 12: SIM8200A-M2 5G Hat

Waveshare SIM8200A-M2 5G Hat, illustrated in Figure 26 is an extension board designed for Raspberry Pi devices extending their capabilities in terms of connectivity. The 5G Hat is compatible with 3G/4G/5G frequency bands of all major countries and regions while also supports standalone and non-standalone 5G implementations. In terms of operating system compatibility SIM8200A-M2 is compatible with all major Linux distributions, Apple iOS and Microsoft Windows. SIM8200A-M2 can operate as a 5G router/access point or as a user equipment (phone calls and SMS) demonstrating superior flexibility with respect to applications and scenarios such (but not limited to) Smart Cities, Robotics and extending network coverage through 5G and security.

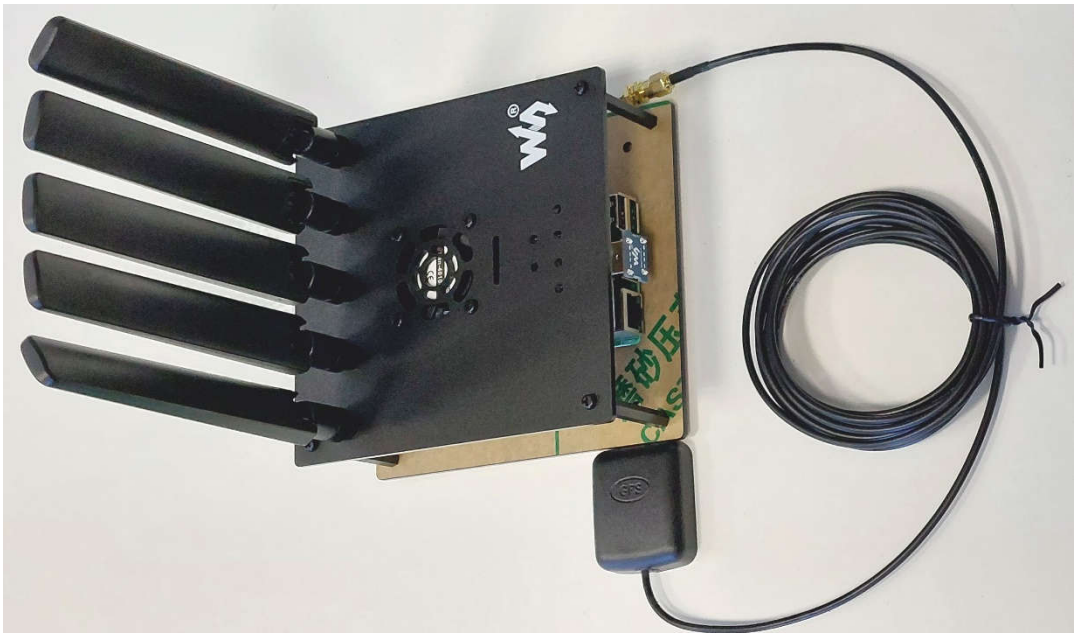

Figure 26: Waveshare SIM8200A-M2 5G Hat for RaspberryPi

In addition, the table belowTable 13 summarizes the 5G module's capabilities.

Table 14: SIMCom SIM8200EA-M2 5G Module Features

SIMCom SIM8200EA-M2 5G Module	
Frequency Bands	Sub-6G (5G-SA & 5G-NSA)
Multiplexing Mode	TDD and FDD
Data rates	2.4 Gbps DL / 500 Mbps UL in 5G-SA/NSA 1 Gbps DL / 200 Mbps UL in LTE
Software Compatibility	Windows/Linux/Android Operating Systems
Hardware Information	SIM card 1.8V/3.0V Antenna connector:6x IPEX-4 connector Passive GPS Antenna

Appendix 13: Xiaomi 11 Lite 5G NE Mobile Phone

Xiaomi 11 Lite 5G NE, illustrated in Figure 27: Xiaomi 11 Lite 5G NE Mobile Phone, is an Android 11 based smartphone device designed and manufactured by the Chinese company Xiaomi and released in September 2021. The smartphone is equipped with a Qualcomm Snapdragon 778G 5G 8 core CPU, 8GBs or memory and 128GB of internal storage. Xiaomi 11 Lite 5G is a solid option to validate connectivity and experiment with thanks to its affordable price and wide range of connectivity technologies (4G/5G). Table 15: Xiaomi 11 Lite 5G NE Mobile Phone specifications depicts the most important technical specifications of the device for the NANCY project.

Figure 27: Xiaomi 11 Lite 5G NE Mobile Phone

Table 15: Xiaomi 11 Lite 5G NE Mobile Phone specifications

Network Techologies	GSM/HSPA/LTE/5G Wi-Fi 802.11 a/b/g/n/ac/6
Hardware features	Qualcomm SM7325 Snapdragon 778G 5G Octa-core CPU 8 GB RAM 128 GB ROM
Network Techologies	GSM/HSPA/LTE/5G Wi-Fi 802.11 a/b/g/n/ac/6

Appendix 14: Sysmocom sysmoISIM-SJA2

The sysmoISIM-SJA2 is subscriber identity module (SIM) card that is compliant with 3GPP/ETSI specifications and facilitates the development of applications utilizing mobile networks. The card comes in four form-factors, namely standard SIM, mini-SIM, micro-SIM, and nano SIM. Furthermore, the SIM card is fully programmable as all its contents and parameters can be modified using a SIM card reader/writer, while the PySim software suite is used for programming the SIM card. A Sysmocom SIM card is shown in Figure 28.

Figure 28: Sysmocom SIM card

Appendix 15: Kingston ValueRAM - DDR4

The ValueRAM's KVR32S22S8/16 is a 2G x 64-bit (16GB) DDR4-3200 CL22 SDRAM (Synchronous DRAM), 1Rx8, non-ECC, memory module, based on eight 2G x 8-bit FBGA components. The SPD is programmed to JEDEC standard latency DDR4-3200 timing of 22-22-22 at 1.2V. This 260-pin DIMM uses gold contact fingers.

Figure 29: KVR32S22S8/16 Kingston ValueRAM - DDR4

The specifications are demonstrated as follows:

Table 16: Specifications of KVR32S22S8/16 Memory module

KVR32S22S8/16 Memory module specifications	
CL(IDD)	22 cycles
Row Cycle Time (tRCmin)	45.75ns(min.)
Refresh to Active/Refresh Command Time (tRFCmin)	350ns(min.)
Row Active Time (tRASmin)	32ns(min.)
UL Rating	94 V - 0
Operating Temperature	0° C to +85° C
Storage Temperature	-55° C to +100° C

The main features are the following:

- Power Supply: VDD = 1.2V Typical
- VDDQ = 1.2V Typical
- VPP = 2.5V Typical

- VDDSPD = 2.2V to 3.6V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self-refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die VREFDQ generation and calibration
- Single-rank
- On-board I2 serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Fly-by topology
- Terminated control command and address bus
- PCB: Height 1.18” (30.00mm)
- RoHS Compliant and Halogen-Free

Appendix 16: Samsung PM9A1 MZVL2512HCJQ - SSD

The Samsung “PM9A1 MZVL2512HCJQ - SSD - 512 GB - PCIe 4.0 x4 (NVMe)” is a solid-state drive in the M.2 2280 form factor. With the rest of the system, the Samsung PM9A1 interfaces using a PCI-Express 4.0 x4 connection. The SSD controller is the Elpis (S4LV003) from Samsung. Samsung has installed 128-layer TLC NAND flash on the PM9A1, the flash chips are made by Samsung. To improve write speeds, a pseudo-SLC cache is used, so bursts of incoming writes are processed more quickly. The cache is sized at 94 GB, once it is full, writes complete at 1000 MB/s. Thanks to support for the fast PCI-Express 4.0 interface, performance is excellent. The PM9A1 is rated for sequential read speeds of up to 6,900 MB/s and 5,000 MB/s write; random IOPS reach up to 800K for reads and 800K for writes.

Figure 30: Samsung PM9A1 MZVL2512HCJQ - SSD - 512 GB - PCIe 4.0 x4 (NVMe)

At the Table 17: SAMSUNG SSD PM9A1 M.2 NVMe 512GB specifications below, the specifications are summarized as follows:

Table 17: SAMSUNG SSD PM9A1 M.2 NVMe 512GB specifications

SAMSUNG SSD PM9A1 M.2 NVMe 512GB	
Model	PM9A1
Interface	PCIe 4.0 x4
Form Factor	M.2
Capacity	512 GB
Sequential Read	6900 MB/s
Sequential Write	5000 MB/s
Random Read	800K IOPS
Random Write	800K IOPS